De la micro a la nanoelectrònica: “there’s plenty of room at the bottom”

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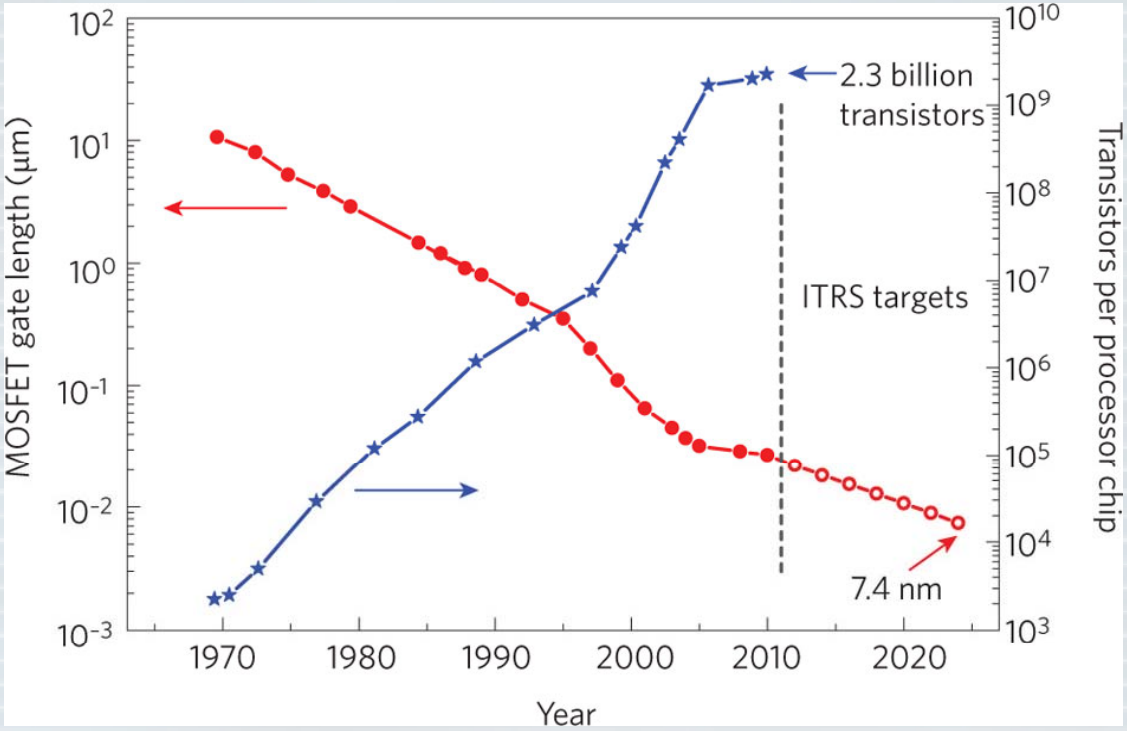
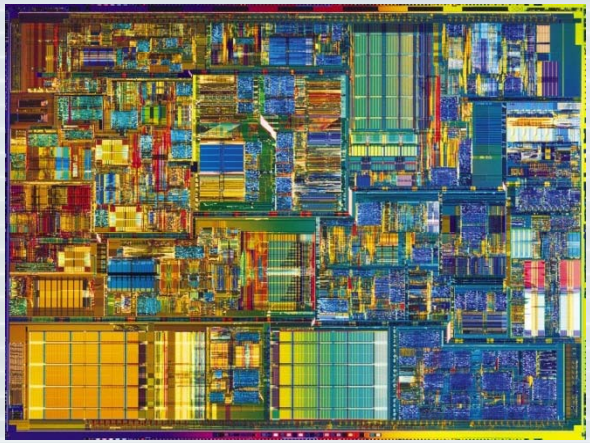
Outline

- Microelectronics at a glance
  - Moore's law and integrated circuits
  - MOS capacitor as a building block for making transistors
  - Transistors as a building block of integrated circuits
  - Transistors in digital electronics
  - Transistor non-idealities
  - Scaling trends of microelectronics
- The path towards nanoelectronics
  - Using quantum effects: the tunnel field-effect transistor
  - Using 1D materials: carbon nanotube transistors
  - Using 2D materials: graphene transistors

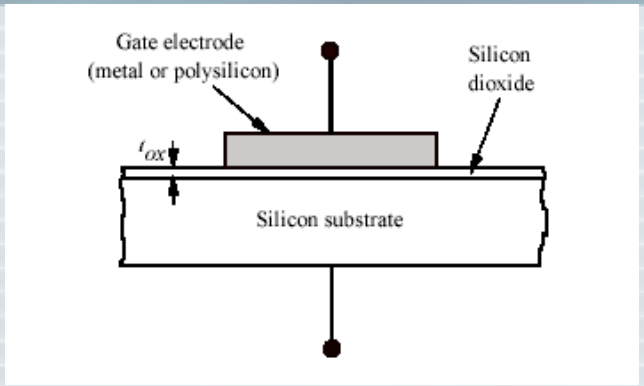




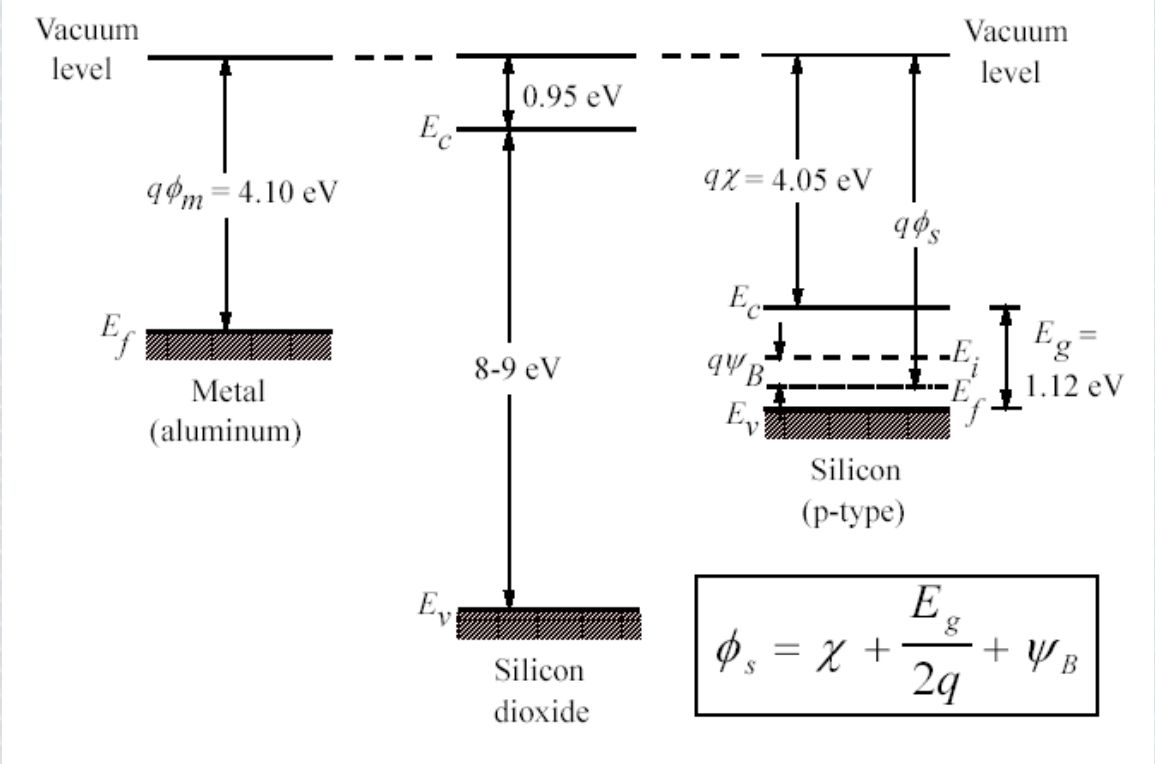
Pentium 4 processor

Evolution of MOSFET gate length in production-stage integrated circuits (filled red circles) and International Technology Roadmap for Semiconductors (ITRS) targets (open red circles). As gate lengths have decreased, the number of transistors per processor chip has increased (blue stars). Maintaining these trends is a significant challenge for the semiconductor industry, which is why new materials such as graphene are being investigated.

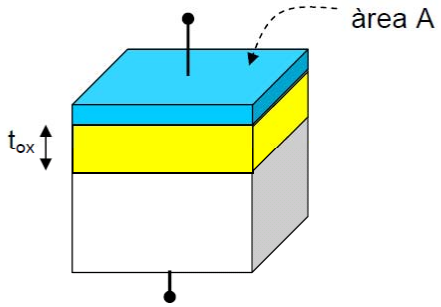
MOS capacitor as a bulding block for transistors



MOS structure



Si l'elèctrode inferior fos un conductor, tindríem un condensador de plaques paral·leles:



La capacitat és en aquest cas:

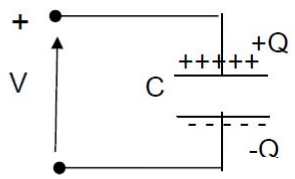
$$C = \frac{\varepsilon_0 \, \varepsilon_{ox}}{t_{ox}} A$$

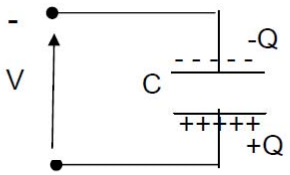
on ε_0 és la constant dielèctrica del buit, i ε_{ox} és la constant dielèctrica relativa del l'òxid.

La capacitat per unitat d'àrea és : $C_{ox} \equiv \frac{\varepsilon_0 \, \varepsilon_{ox}}{t_{ox}}$

Sabem que la càrrega que amagatzema el condensador és la capacitat multiplicada per la diferència de pòtencial que se li aplica, amb el signe corresponent:

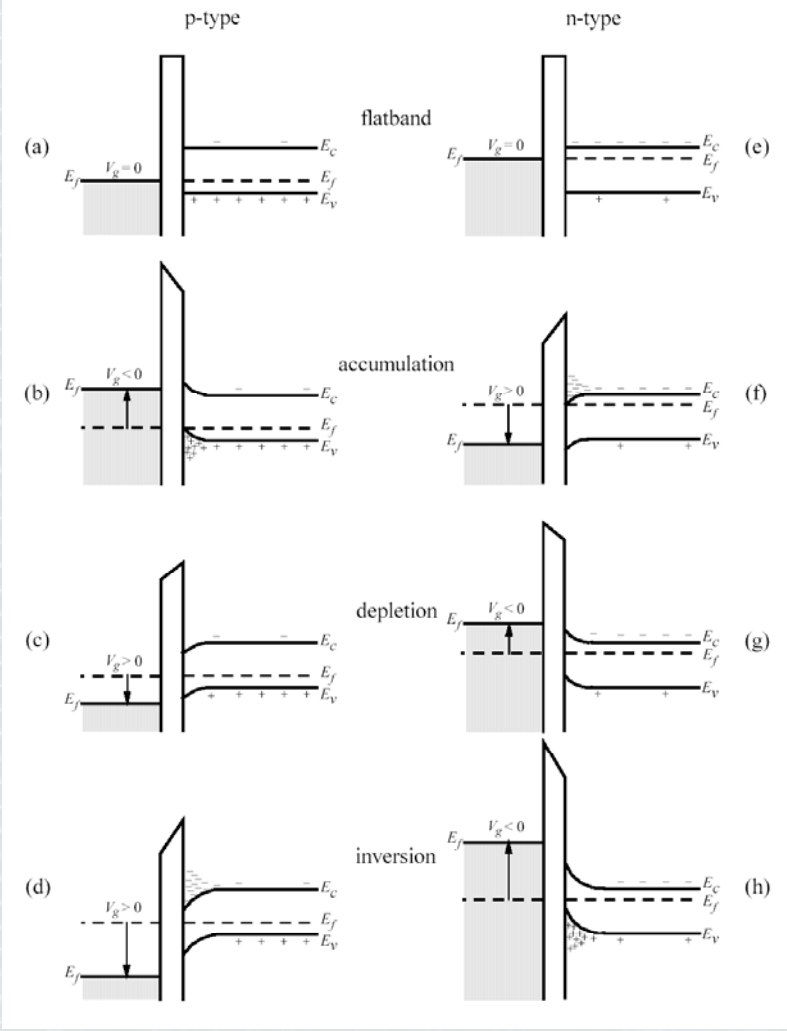
$$Q = C \, V$$



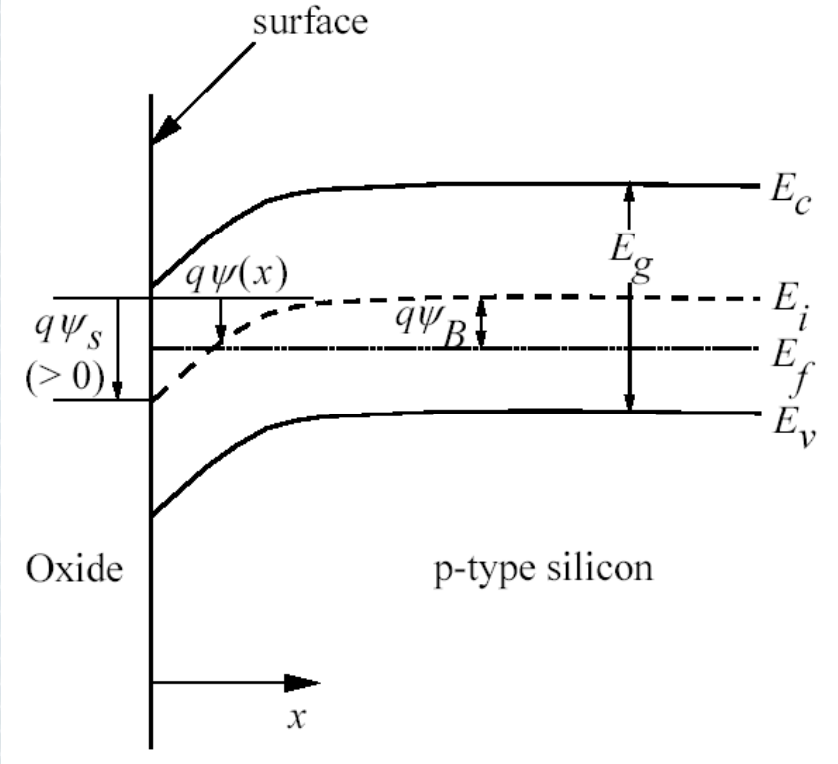


Accumulation, depletion, and inversion

Assume: $\phi_m = \phi_s$



Poisson's equation



$$\frac{d^2\psi}{dx^2} = -\frac{d\mathcal{E}}{dx} = -\frac{q}{\varepsilon_{si}}\left[p(x) - n(x) + N_d^{+}(x) - N_a^{-}(x)\right]$$

$$p(x) = n_i e^{q(\psi_f - \psi_i)/kT} = n_i e^{q(\psi_B - \psi)/kT} = N_a e^{-q\psi/kT}$$

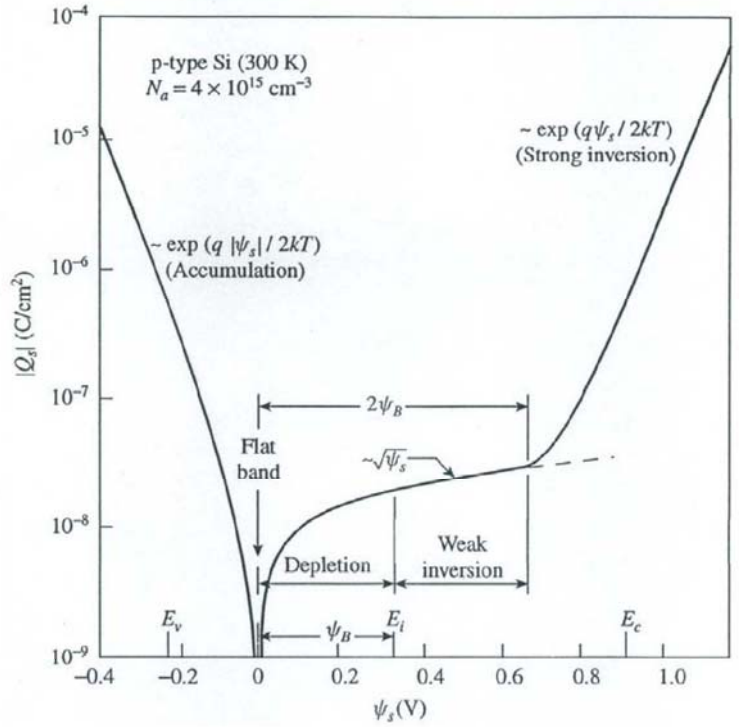
$$n(x) = n_i e^{q(\psi_i - \psi_f)/kT} = n_i e^{q(\psi - \psi_B)/kT} = \frac{n_i^2}{N_a} e^{q\psi/kT}$$

$$\frac{d^2\psi}{dx^2} = -\frac{q}{\varepsilon_{si}}\left[N_a\left(e^{-q\psi/kT} - 1\right) - \frac{n_i^2}{N_a}\left(e^{q\psi/kT} - 1\right)\right]$$

Solving Poisson's equation

$$\mathcal{E}^2(x) = \left(\frac{d\psi}{dx}\right)^2 = \frac{2kTN_a}{\varepsilon_{si}}\left[\left(e^{-q\psi/kT} + \frac{q\psi}{kT} - 1\right) + \frac{n_i^2}{N_a^2}\left(e^{q\psi/kT} - \frac{q\psi}{kT} - 1\right)\right]$$

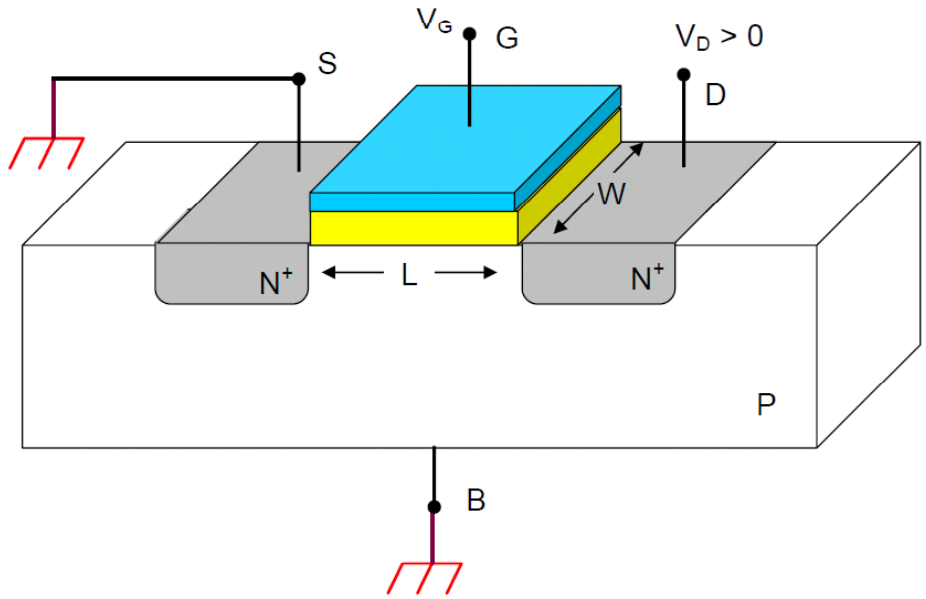
$$Q_s = -\varepsilon_{si}\mathcal{E}_s = \pm\sqrt{2\varepsilon_{si}kTN_a}\left[\left(e^{-q\psi_s/kT} + \frac{q\psi_s}{kT} - 1\right) + \frac{n_i^2}{N_a^2}\left(e^{q\psi_s/kT} - \frac{q\psi_s}{kT} - 1\right)\right]^{1/2}$$



Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET): basis

Un transistor MOS està format per una estructura MOS a la que s'afegeixen dues regions per a donar i recollir electrons o forats (segons el tipus de semiconductor que sigui).

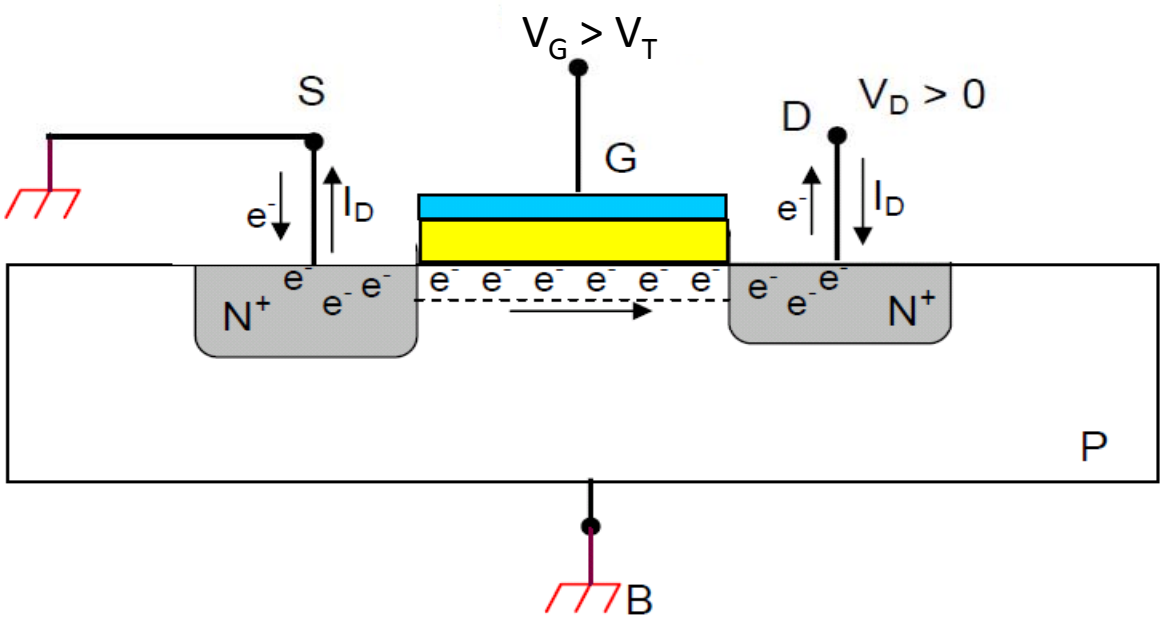
Com a exemple veurem el que s'anomena MOSFET de canal N:



Els quatre terminals s'anomenen:

- Font (ó sortidor) ---> S
- Porta ---> G
- Drenador ---> D
- Substrat ---> B

Si $V_{GS}>V_T$ es forma un "canal" d'electrons entre la font i el drenador, que permeten el pas d'electrons d'una part a l'altre (si $V_{DS} > 0$):



Per tant:

- quan $V_{GS}>V_T$, es forma un canal d'electrons que fa que passi corrent elèctric del drenador D a la font S.

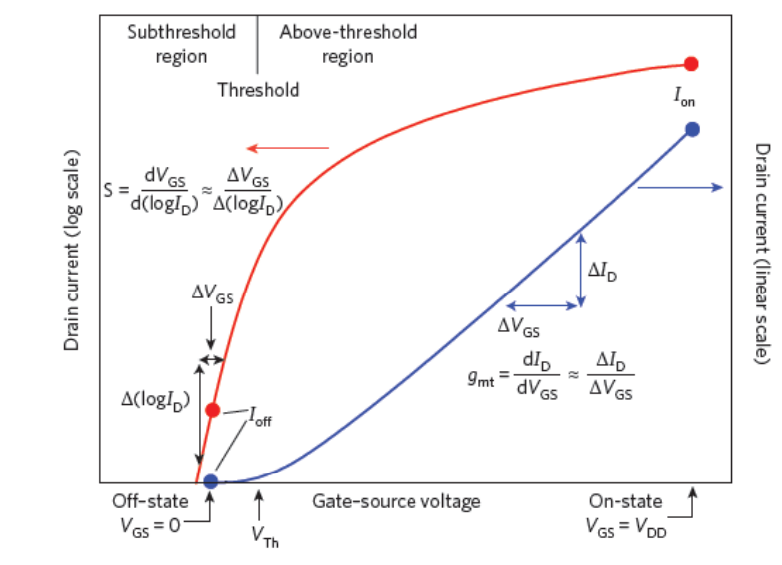
- quan $V_{GS}<V_T$, no hi ha canal, per tant NO passa corrent elèctric del drenador D a la font S.

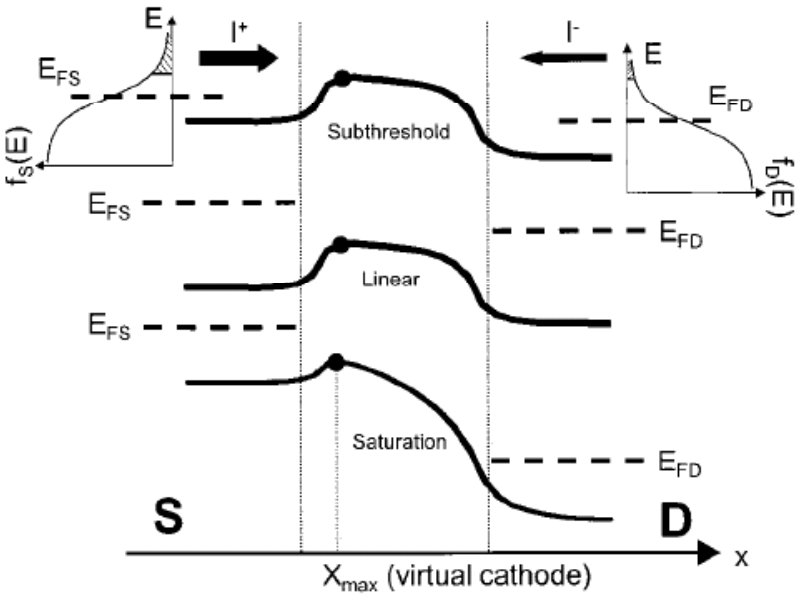
El transistor MOS es comporta doncs com un interruptor.

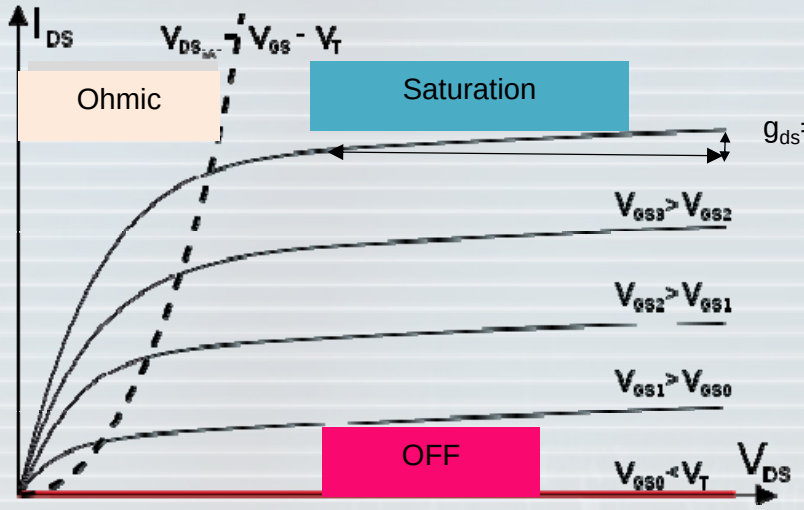
Com hem vist, el comportament del transistor es controla amb el potencial de porta V_{GS}.

Aquest que hem vist es diu **transistor de canal N** perquè el canal que es forma és d'electrons.

El **transistor de canal P** funciona de la mateixa manera, canviant els semiconductors P per N i N per P, canviant els signes dels potencials i canviant electrons per forats i a la inversa.







$g_{ds} = dI_{DS}/dV_{DS}$

Aquestes corbes corresponen a les següents equacions matemàtiques:

Si de finim la tensió de drenador de saturació com: $V_{DS,SAT} = V_{GS} - V_T$,

llavors, si $V_{DS} < V_{DSSAT}$:

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

i si $V_{DS} > V_{DSSAT}$:

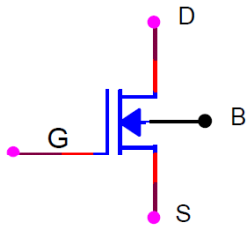
$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\frac{(V_{GS} - V_T)^2}{2}$$

Tipus de transistors MOS

A) Transistors de canal N i de canal P

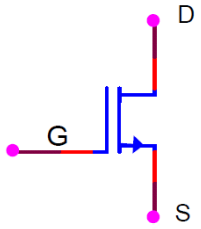
El transistor MOS que hem vist fins ara condueix el corrent elèctric amb electrons. Com ja hem dit, s'anomena **transistor de canal N** o, de manera abreviada, **transistor NMOS**.

En els circuits elèctrics es representa pel següent símbol:



on notem que la fletxa va del substrat P al canal N, és a dir, en el sentit del corrent en el suposat díode "substrat-canal".

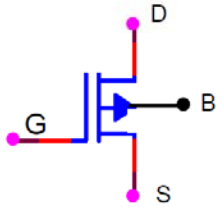
En el cas més normal en que el substrat B està connectat a la font S, es pot fer servir el següent símbol simplificat:



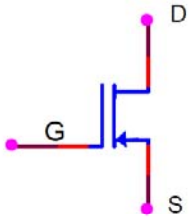
on ara la fletxa va en el sentit del corrent, és a dir, de drenador D a font S.

Transistor de canal P

En els circuits elèctrics es representa amb el símbol:

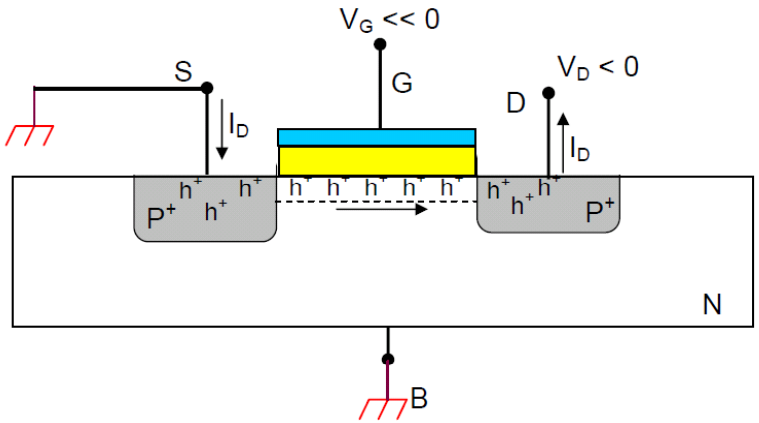


En el cas més normal en que el substrat B està connectat a la font S, es pot fer servir el següent símbol simplificat:

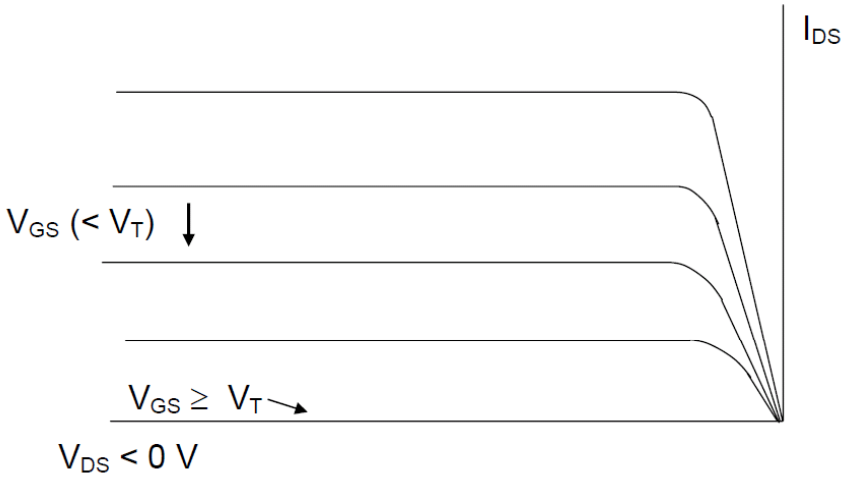


El transistor MOS complementari d'aquest és el que condueix el corrent elèctric amb forats. S'obté canviant el tipus de semiconductor de cada regió i els signes dels potencials. S'anomena **transistor de canal P** o, de manera abreviada, **transistor PMOS**.

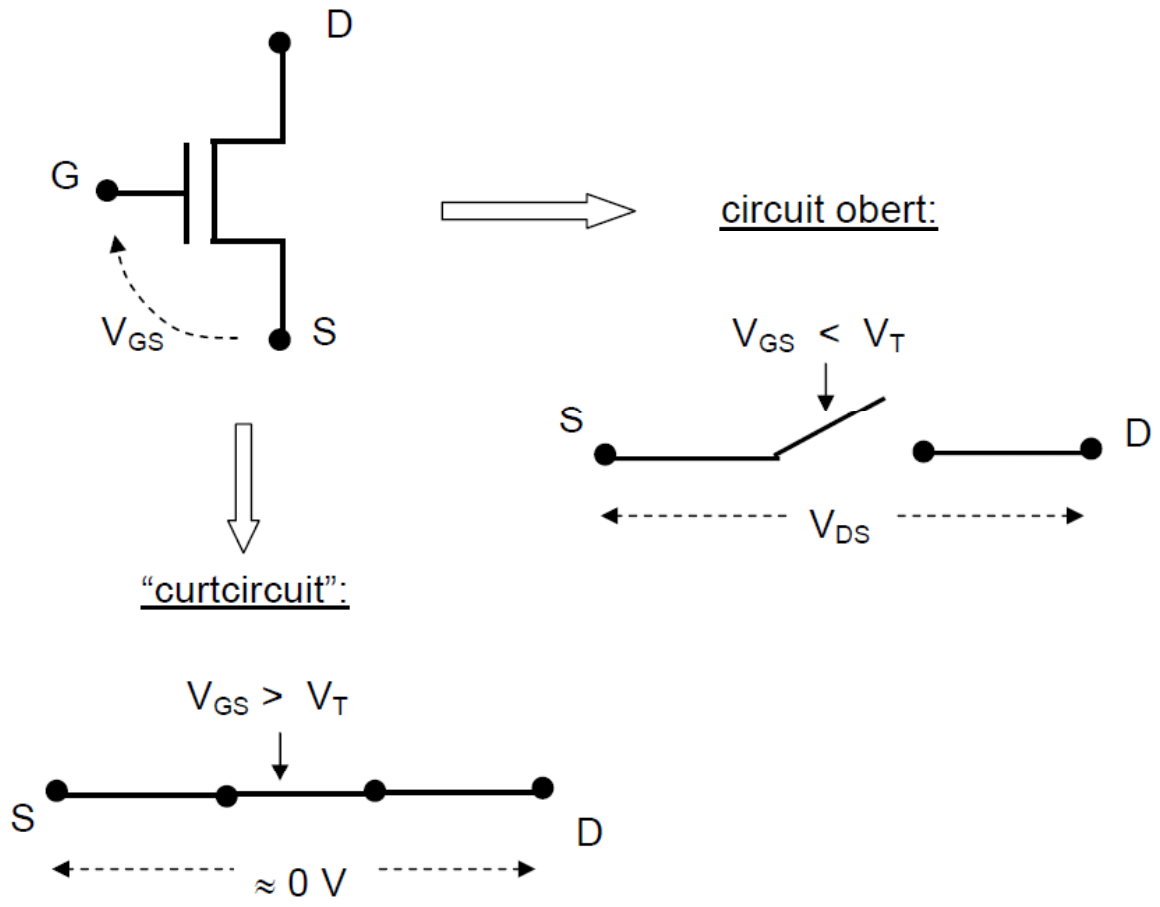
La seva estructura és:



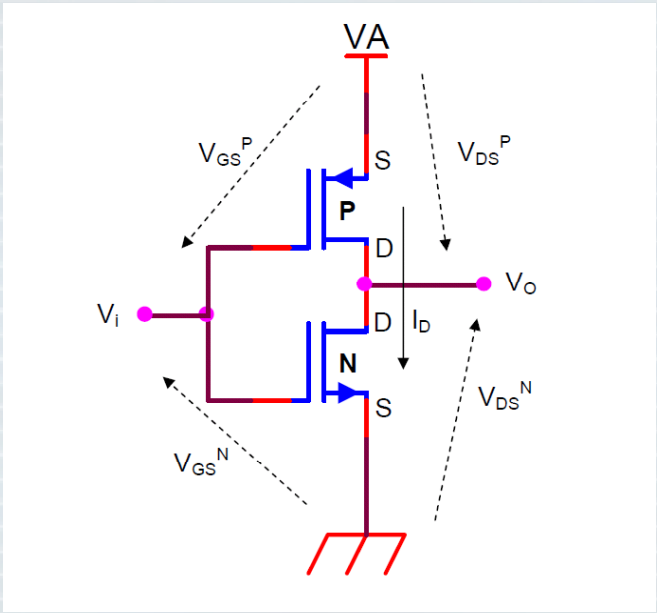
$V_T < 0$)



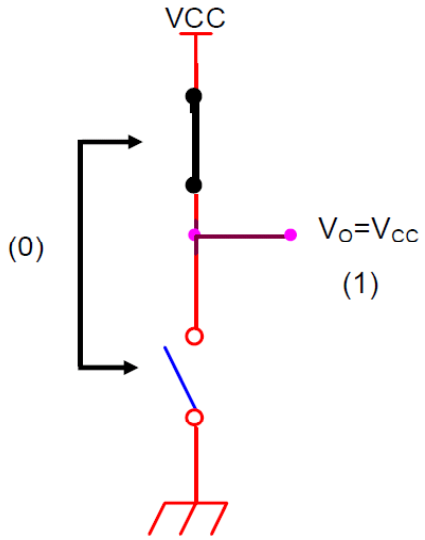
Field-effect transistor applications in digital electronics

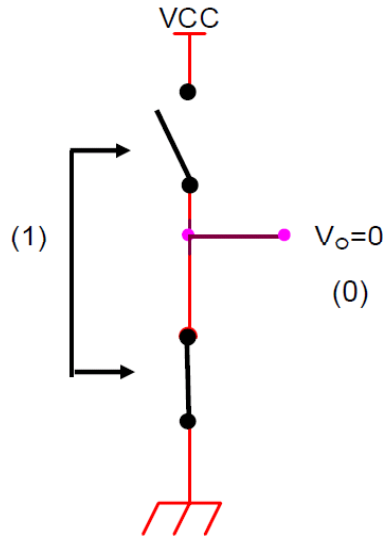

D
G
S
V_{GS}
circuit obert:
V_{GS} < V_T
S
D
V_{DS}
"curtcircuit":
V_{GS} > V_T
S
D
≈ 0 V

Inversor CMOS



El funcionament qualitatiu de l'inversor CMOS es pot explicar a partir de dos interruptors posats en sèrie, que funcionen de manera que quan un s'obre l'altre es tanca:

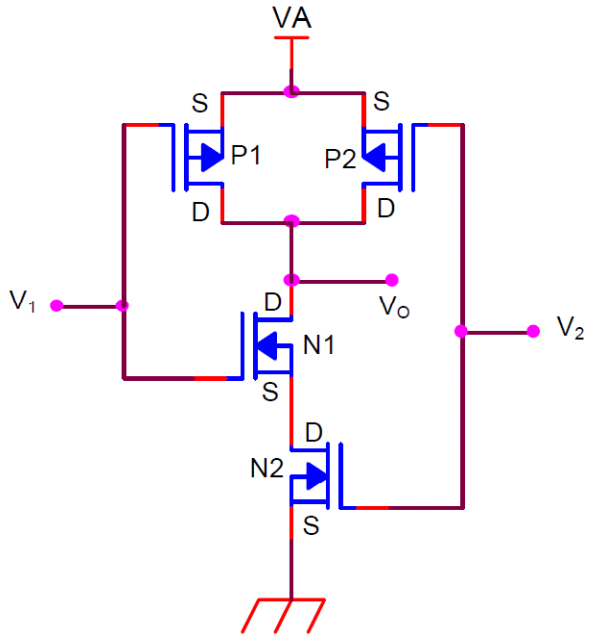




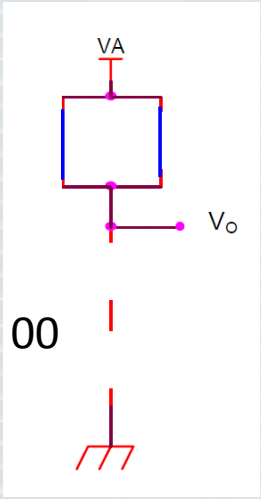
Amb aquesta configuració, en cap dels dos estats lògics hi ha un corrent entre la font de tensió V_{CC} i "terra". Per tant el circuit **no consumeix corrent** mentre està en un estat lògic definit.

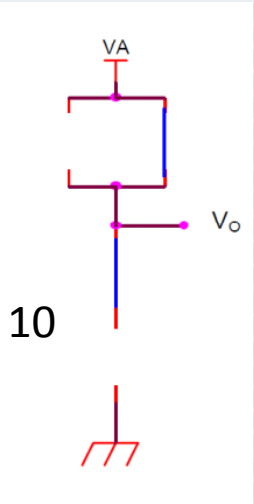
Porta NAND CMOS

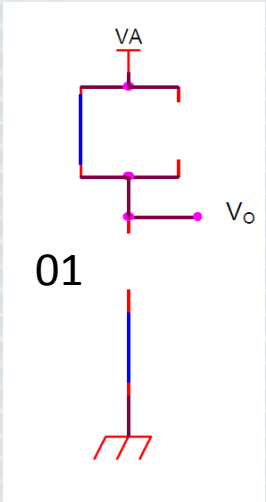
Una porta NAND (No-I) CMOS de dues entrades correspon al següent circuit.

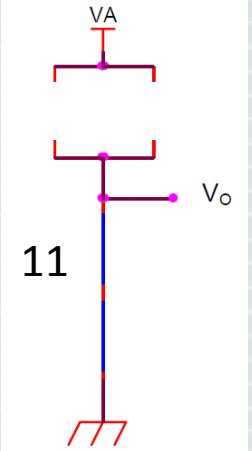


Entrada 1	Entrada 2	Sortida
0	0	1
0	1	1
1	0	1
1	1	0

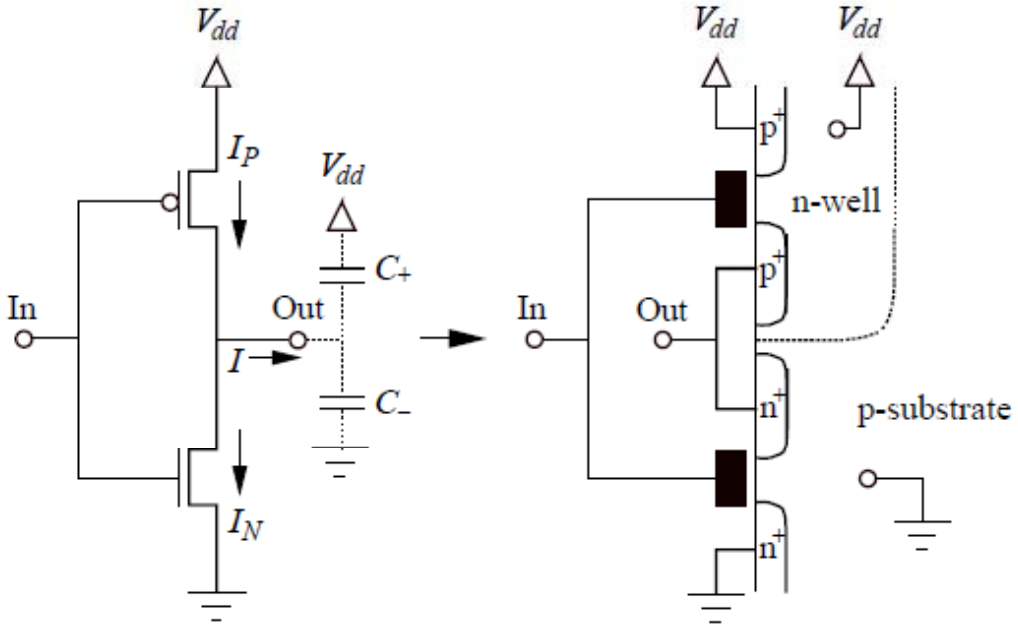






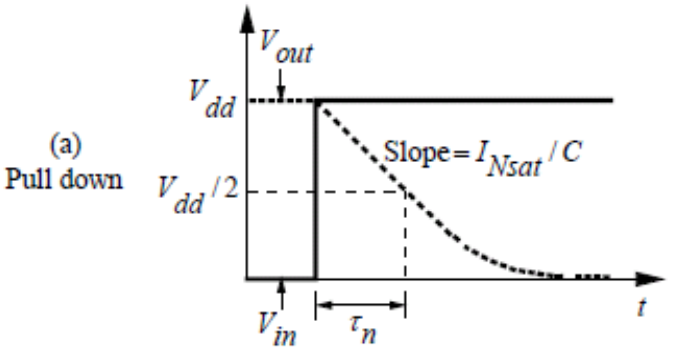


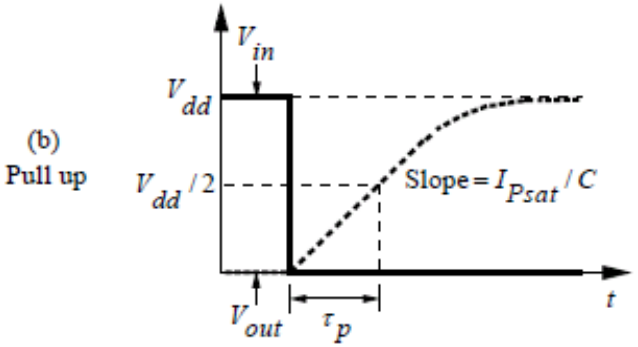
CMOS Inverter



Since only one of the transistors is on in the steady state, there is no static current or static power dissipation in a CMOS inverter.

Switching Waveform for a Step Input





For nMOSFET pull down transition,

$$(C_- + C_+)\frac{dV_{out}}{dt} = C\frac{dV_{out}}{dt} = -I_N(V_{in} = V_{dd})$$

The pull down delay is

$$\tau_n = \frac{CV_{dd}}{2I_{Nsat}} = \frac{CV_{dd}}{2W_n I_{nsat}}$$

Similarly, the pMOSFET pull up delay is

$$\tau_p = \frac{CV_{dd}}{2I_{Psat}} = \frac{CV_{dd}}{2W_p I_{psat}}$$

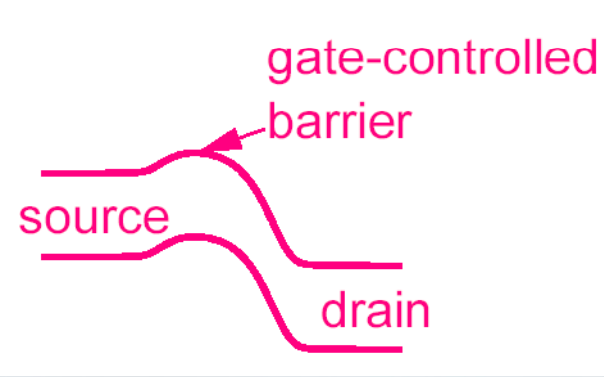
Field-effect transistors: non-idealities

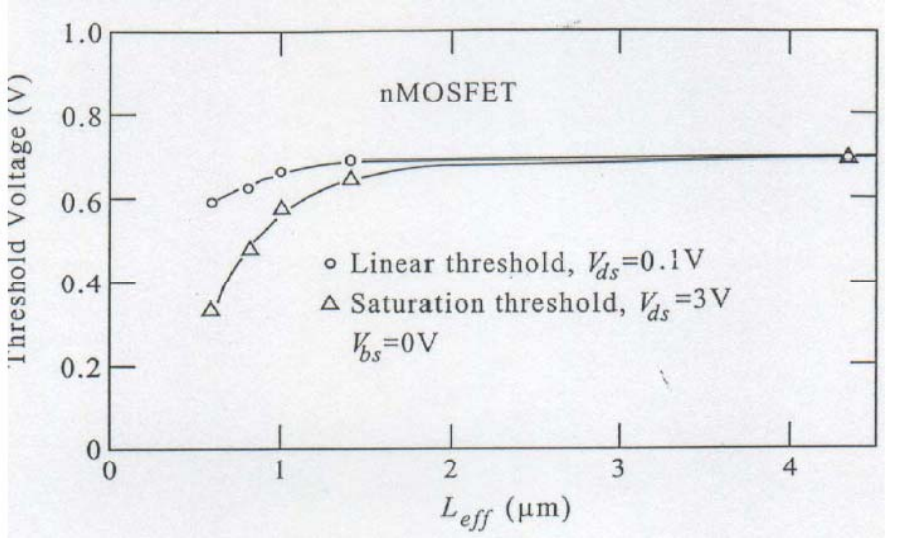
Short-channel MOSFET

If $L \downarrow,\ I_{ds} = I_{dsat} = \mu_{eff} C_{ox} \frac{W}{L} \frac{(V_g - V_t)^2}{2m} \uparrow$

and $C_g = \frac{2}{3} WLC_{ox} \downarrow.$

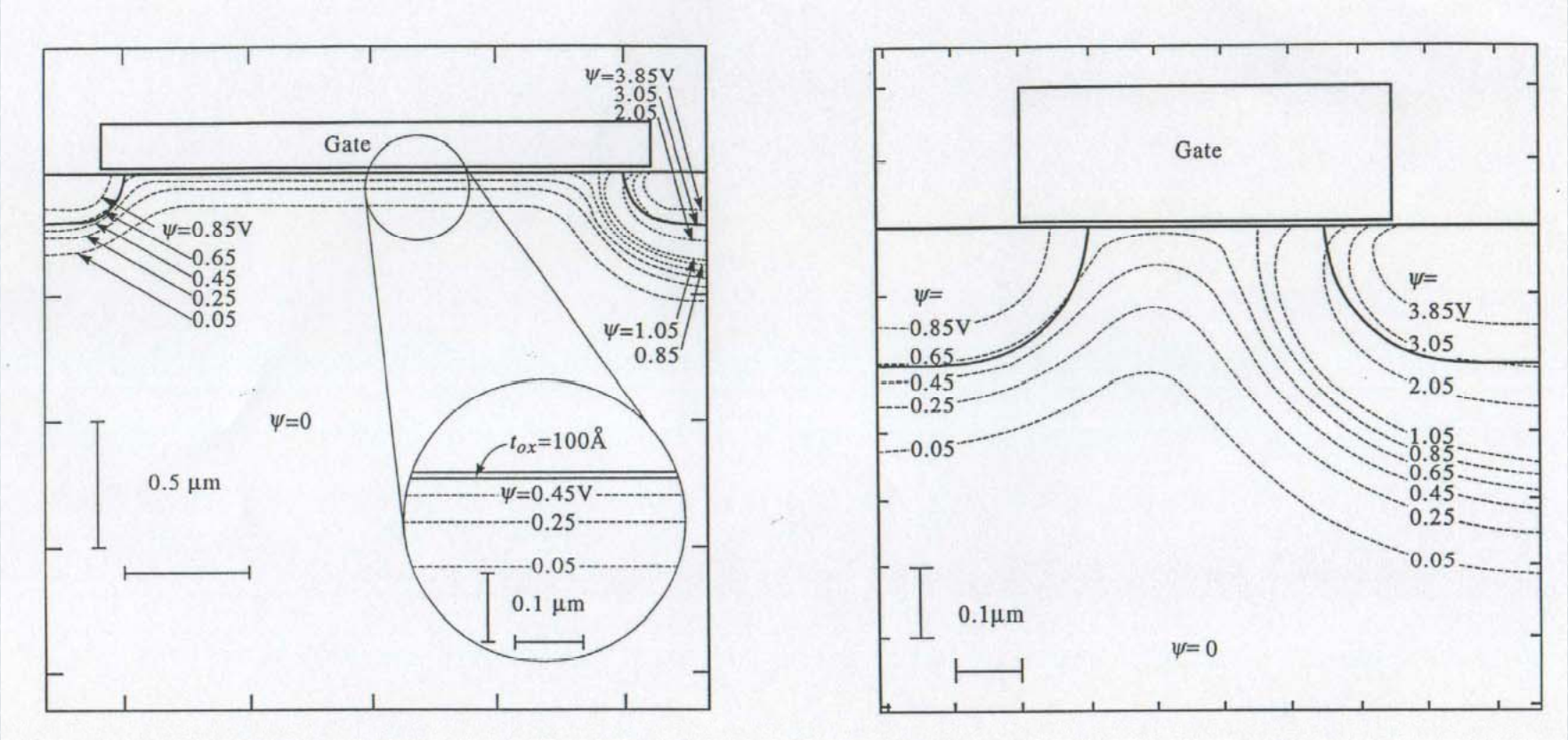
Threshold voltage becomes sensitive to the channel length and drain bias





2D potential-contours

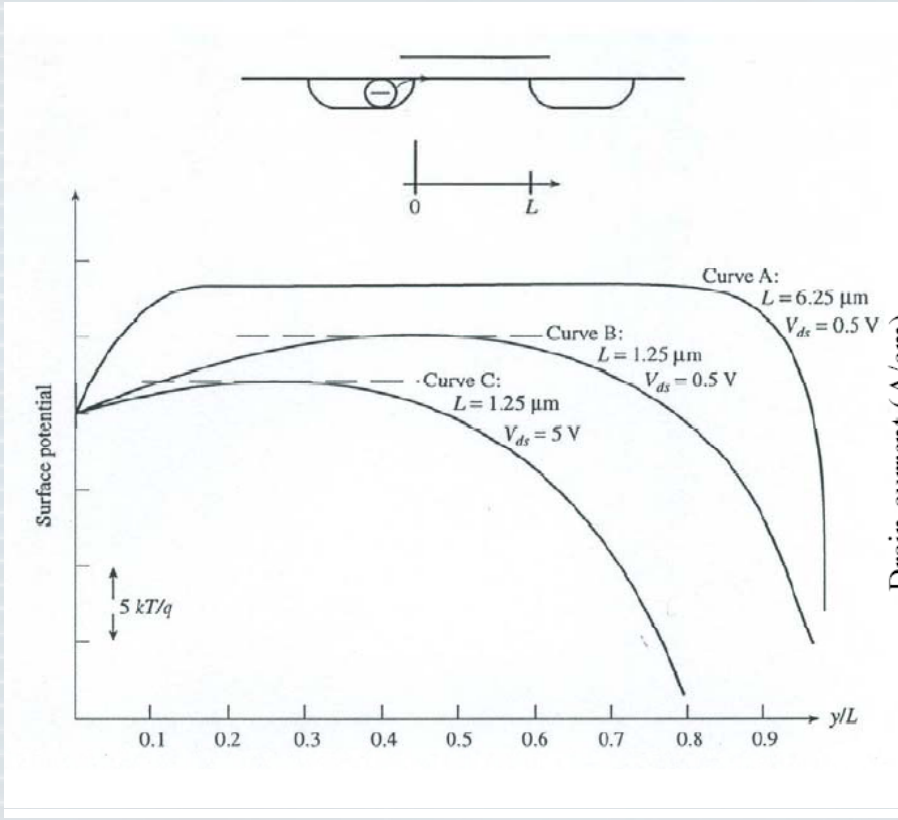
(Same gate voltage)

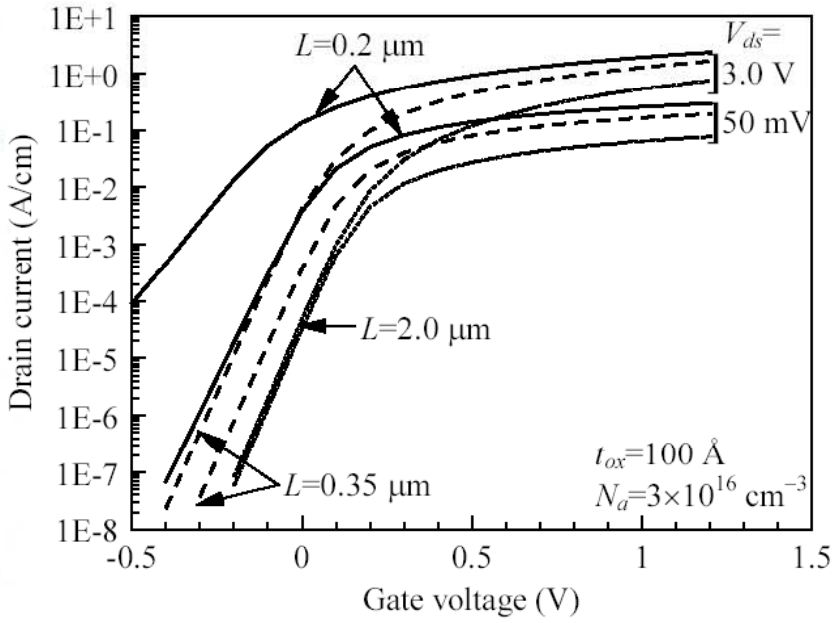


Long-channel

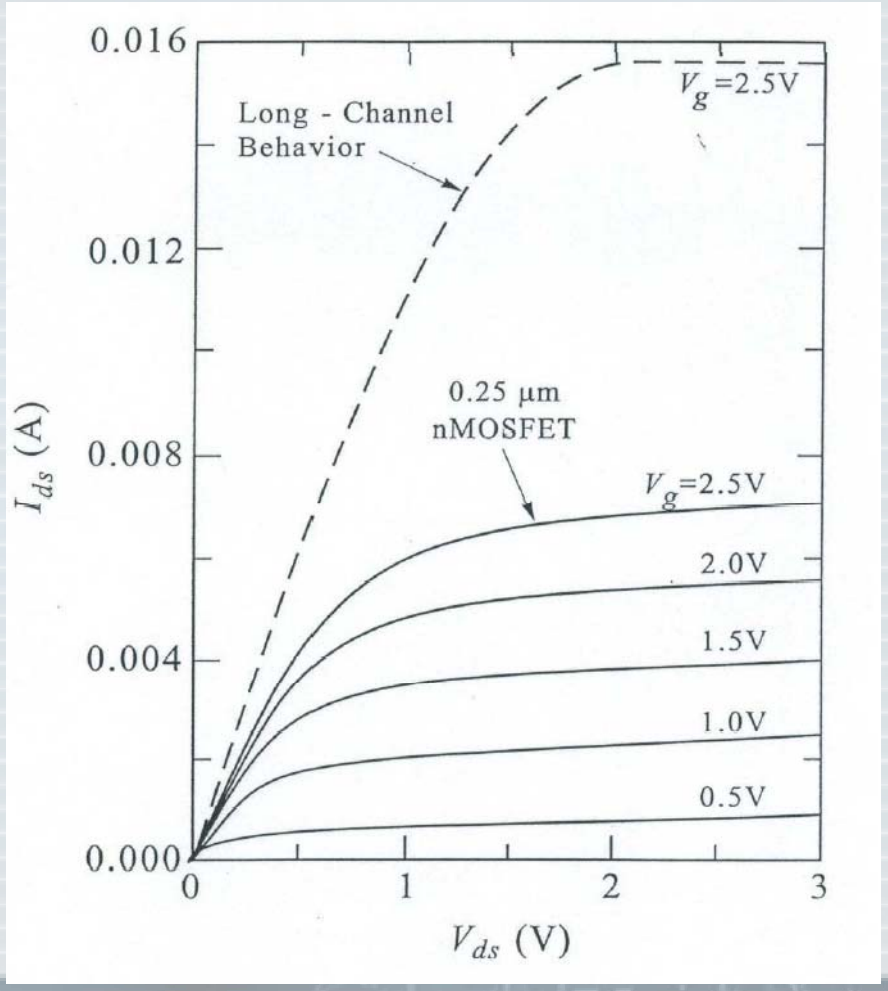
Short-channel

Drain-Induced Barrier Lowering (DIBL)





Velocity saturation



* Because of velocity saturation, the saturation of drain current in a short channel device occurs at a much lower voltage than $V_{dsat}=(V_g-V_t)/m$ for long-channel MOSFETs.

- This causes the saturation current, I_{dsat} , to deviate from the $\propto (V_g-V_t)^2$ behavior and 1/L dependence.

Microelectronics evolution is based on MOSFET scaling

MOSFET Scaling

Device scaling: Simplified design goals/guidelines for shrinking device dimensions to achieve density and performance gains, and power reduction in VLSI.

Issues: Short-channel effect, Power density, Switching delay, Reliability.

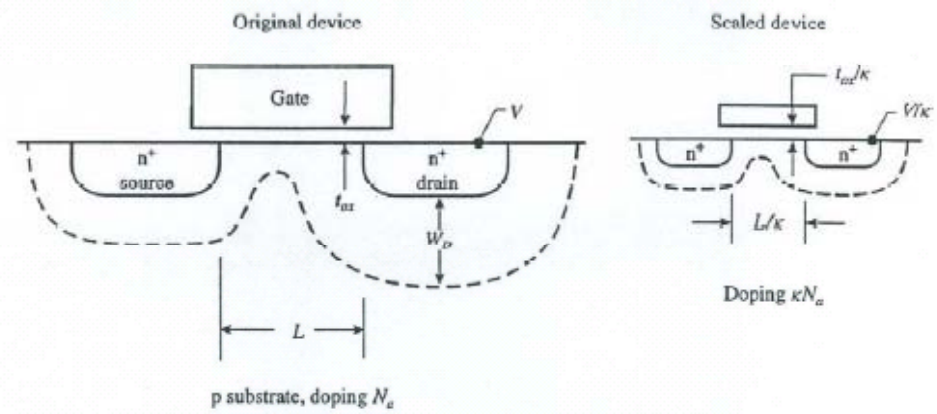


FIGURE 4.1. Principles of MOSFET constant-electric-field scaling. (After Dennard, 1986.)

The principle of constant-field scaling lies in scaling the device voltages and the device dimensions (both horizontal and vertical) by the same factor, κ (> 1), such that the electric field remains unchanged.

Rules of Constant Field Scaling

	MOSFET Device and Circuit Parameters	Multiplicative Factor ($\kappa > 1$)
Scaling assumptions	Device dimensions (t_{ox}, L, W, x_j)	$1/\kappa$
	Doping concentration (N_a, N_d)	κ
	Voltage (V)	$1/\kappa$
Derived scaling behavior of device parameters	Electric field (E)	1
	Carrier velocity (v)	1
	Depletion layer width (W_d)	$1/\kappa$
	Capacitance ($C = \varepsilon A/t$)	$1/\kappa$
	Inversion layer charge density (Q_i)	1
	Current, drift (I)	$1/\kappa$
	Channel resistance (R_{ch})	1
Derived scaling behavior of circuit parameters	Circuit delay time ($\tau \sim CV/I$)	$1/\kappa$
	Power dissipation per circuit ($P \sim VI$)	$1/\kappa^2$
	Power-delay product per circuit ($P \times \tau$)	$1/\kappa^3$
	Circuit density ($\propto 1/A$)	κ^2
	Power density (P/A)	1

Clever solutions to continue CMOS scaling

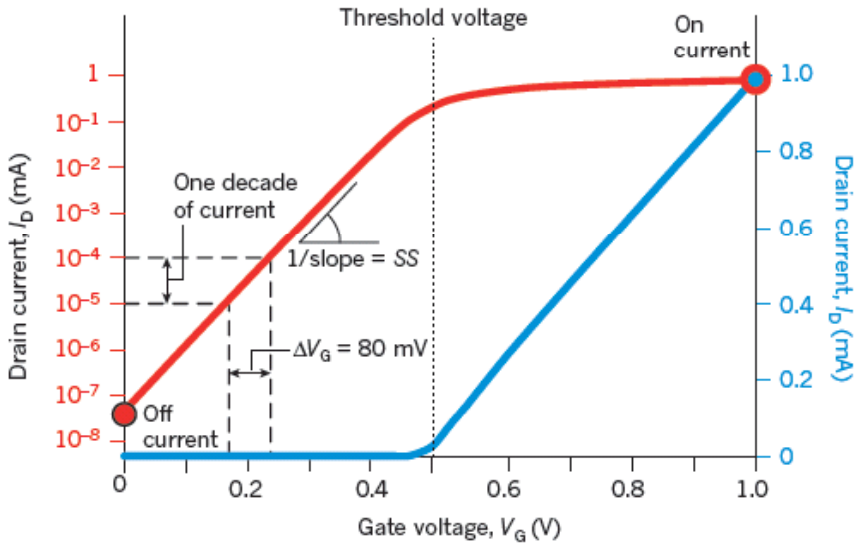


Figure 2 | The drain current as a function of gate voltage in a MOSFET. The two curves show identical data that have been plotted using a linear scale (blue curve; *y* axis, right) and a logarithmic scale (red curve; *y* axis, left). When the gate voltage (V_G) is increased, the number of electrons in the channel increases. This, in turn, increases the current flowing between the source and the drain. The current at the minimum gate voltage (0 V) is the off current, and the current at the maximum gate voltage (1 V in this case) is the on current. Above the threshold voltage (dashed line), the drain current (I_D) increases linearly. Below the threshold voltage, the drain current increases exponentially with the gate voltage. The slope of this exponential increase on a logarithmic scale is called the subthreshold slope (*SS*) and is expressed in millivolts per decade of current. Therefore, if the subthreshold slope is 80 mV decade^{-1}, for example, the gate voltage needs to be increased by 80 mV to increase the subthreshold current by tenfold.

Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors

Isabelle Ferain, Cynthia A. Colinge & Jean-Pierre Colinge

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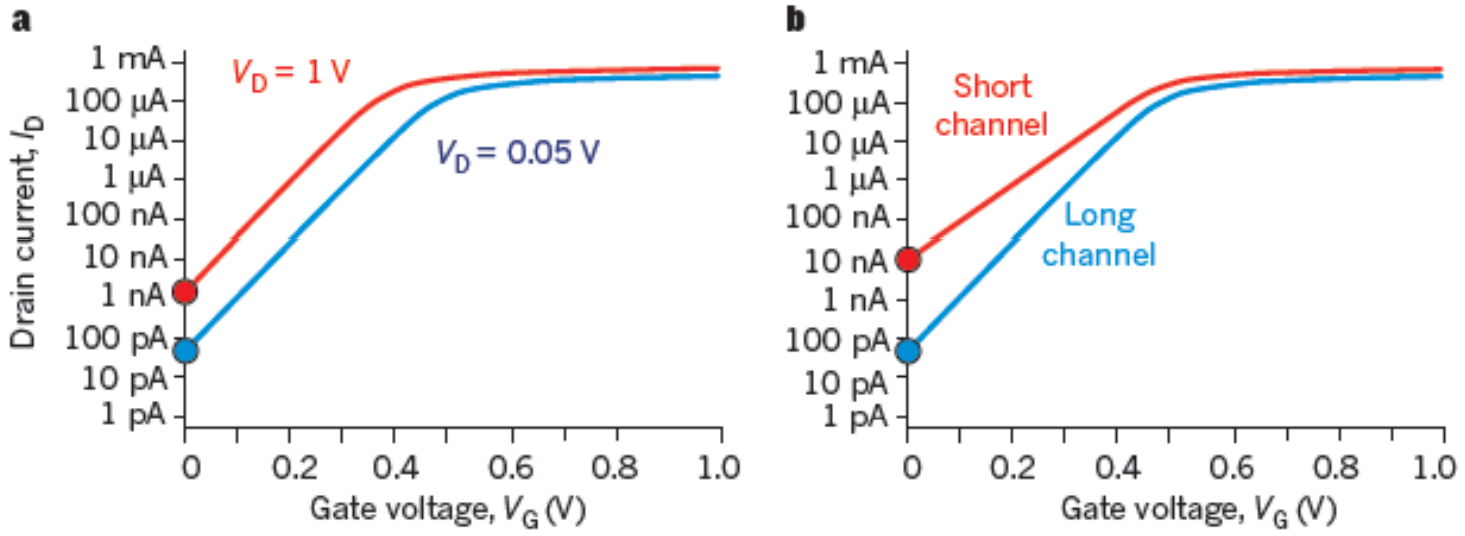

Figure 4 | Illustration of short-channel effects. The blue curves show the relationship between the drain current (I_D) and the gate voltage (V_G) when the drain voltage (V_D) is low (0.05 V), and the red curves show the same relationship when the drain voltage is high (1 V). **a**, The DIBL effect shifts the electrical characteristics of the transistor to the left when the drain voltage is increased. This typically occurs when the device needs to be turned off. **b**, The subthreshold slope increases when the channel length is decreased, which slows down the variation of the current with gate voltage that occurs below the threshold voltage. Both of these effects increase the off currents, which are indicated by the blue and red circles.

Multi-gate MOSFET

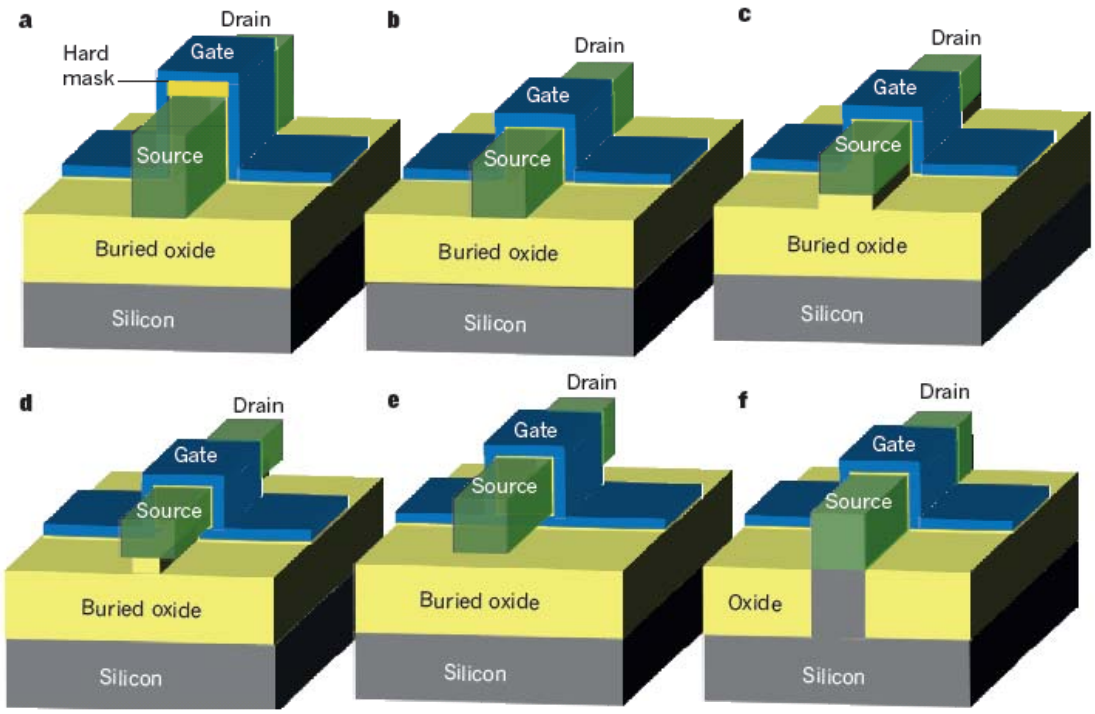

Figure 5 | Types of multigate MOSFET. The different ways in which the gate electrode can be wrapped around the channel region of a transistor are shown. **a**, A silicon-on-insulator (SOI) fin field-effect transistor (FinFET). The 'hard mask' is a thick dielectric that prevents the formation of an inversion channel at the top of the silicon 'fin'. Gate control is exerted on the channel from the lateral sides of the device. **b**, SOI triple-gate (or tri-gate) MOSFET. Gate control is exerted on the channel from three sides of the device (the top, as well as the left and right sides). **c**, SOI Π-gate MOSFET. Gate control is improved over the tri-gate MOSFET shown in **b** because the electric field from the lateral sides of the gate exerts some control on the bottom side of the channel. **d**, SOI Ω-gate MOSFET. Gate control of the bottom of the channel region is better than in the SOI Π-gate MOSFET. The names Π gate and Ω gate reflect the shape of the gates. **e**, SOI gate-all-around MOSFET. Gate control is exerted on the channel from all four sides of the device. **f**, A bulk tri-gate MOSFET. Gate control is exerted on the channel from three sides of the device (the top, the left and the right). In this case, there is no buried oxide underneath the device.

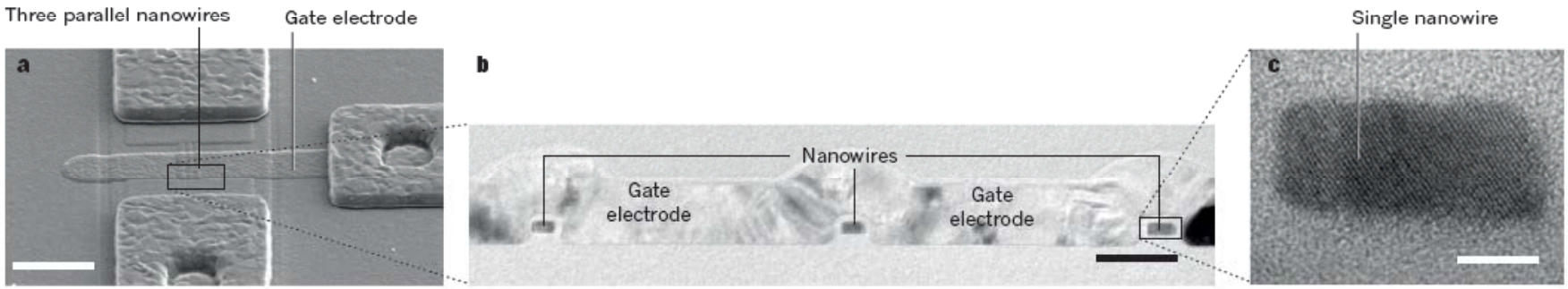

Figure 6 | A multifingered (three-finger) silicon nanowire transistor. **a**, Scanning electron microscopy image of a device with three parallel nanowires that have a common gate electrode. Scale bar, 5 μm. **b**, Transmission electron microscopy image of the three nanowires and the common polysilicon gate electrode in an Ω-gate electrode configuration. Scale bar, 50 nm. **c**, High-resolution transmission electron microscopy image of a nanowire. Scale bar, 5 nm.

Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors

Isabelle Ferain, Cynthia A. Colinge & Jean-Pierre Colinge

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The tunnel effect transitor as an illustrative example of nanoelectronic device taking advantage of quantum effects

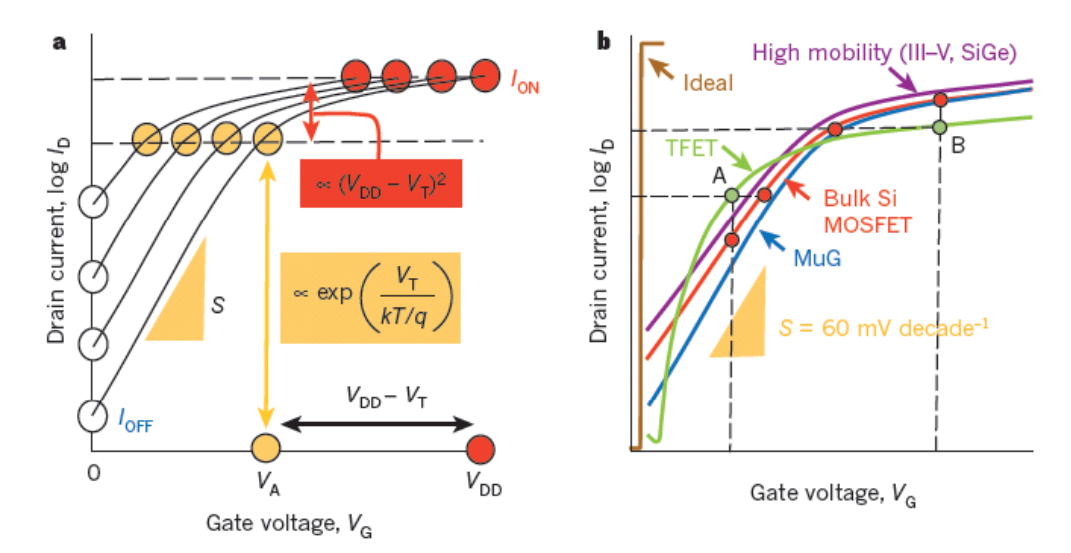

Figure 1 | Power challenge and main characteristics of an energy-efficient tunnel FET. **a**, Transfer characteristics (drain current, I_D, and gate voltage, V_G) of a MOSFET switch showing an exponential increase in I_{OFF} (more than tenfold increase for every 60 mV at room temperature) because of an incompressible subthreshold swing, S. Here the simultaneous scaling down of both the supply voltage, V_{DD}, and the threshold voltage, V_T, maintains the same performance (I_{ON}) by keeping the overdrive ($V_{DD} - V_T$) constant. **b**, Qualitative comparison of three engineering solutions to improve the characteristics of the bulk silicon MOSFET switch (red): a multigate device (MuG, blue) for improved electrostatics; a high-mobility channel (purple) using group III–V and SiGe materials; and a TFET (green), which has a steep off–on transition and the lowest I_{OFF}. At operation point A, because of its subthermal subthreshold swing, the TFET offers not only an improved I_{ON}/I_{OFF} but also a superior performance and a power saving at the same performance as a MOSFET. At operation point B, corresponding to higher performance, the MOSFET switch becomes the better solution. **c**, Comparison of the minimum switching energy, E_{min}, and the corresponding voltage supply, V_{DDmin}, for a subthermal swing device ($S < 60$ mV decade^{-1}, green curve) and the ideal MOSFET ($S = 60$ mV decade^{-1}, red) at the same I_{ON}/I_{OFF}. **d**, Comparison between switching energy and performance for a MOSFET and a TFET. The steep-swing TFET offers better energy efficiency at lower or moderate performance level.

Tunnel field-effect transistors as energy-efficient electronic switches

Adrian M. Ionescu & Heike Riel

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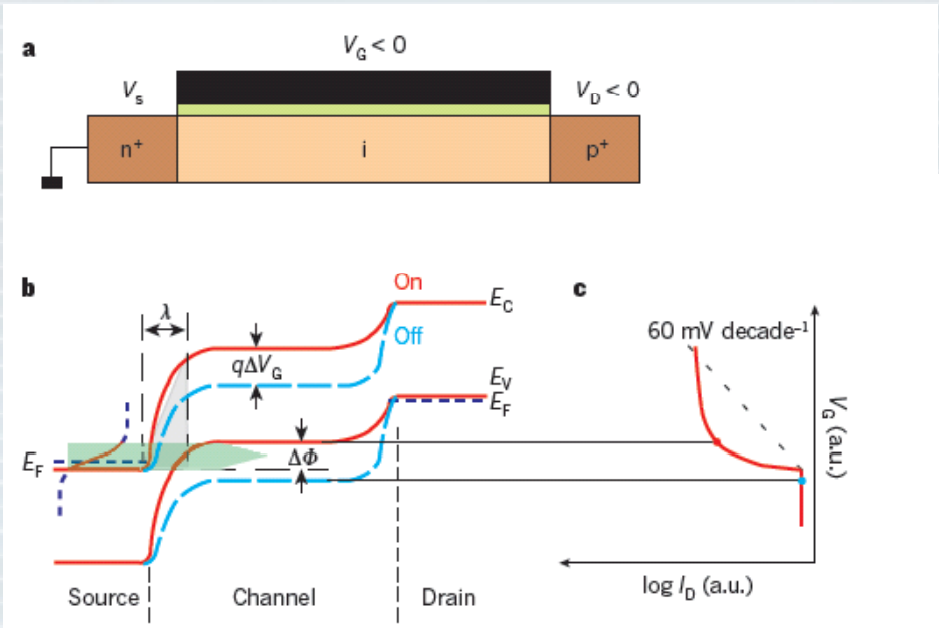

Figure 2 | Principle of operation of a TFET. **a**, Schematic cross-section of p-type TFET with applied source (V_S), gate (V_G) and drain (V_D) voltages. **b**, Schematic energy band profile for the off state (dashed blue lines) and the on state (red lines) in a p-type TFET. In the off state, no empty states are available in the channel for tunnelling from the source, so the off current is very low. Decreasing V_G moves the valence band energy (E_V) of the channel above the conduction band energy (E_C) of the source so that interband tunnelling can occur. This switches the device to the on state, in which electrons in the energy window, $\Delta\Phi$ (green shading), can tunnel from the source conduction band into the channel valence band. Electrons in the tail of the Fermi distribution cannot tunnel because no empty states are available in the channel at their energy (dotted black line), so a slope of less than 60 mV decade^{-1} can be achieved. This is indicated in the schematic transfer characteristics shown in **c**. In contrast to a conventional MOSFET, a TFET has a slope that is not linear on a logarithmic scale, which can be explained by the complex dependency of the tunnel current on the transmission probability through the barrier, as well as on the number of available states determined by the source and channel Fermi functions. The BTBT can be approximated by the triangular potential barrier indicated in grey. Because the tunnel current depends on the transmission probability through the barrier, as well as on the number of available states determined by the source and channel Fermi functions, the resultant slope is not linear on a logarithmic scale, which it is for a conventional MOSFET. λ, screening tunnelling length. a.u., arbitrary units; E_F, Fermi energy.

Tunnel field-effect transistors as energy-efficient electronic switches

Adrian M. Ionescu & Heike Riel

3 3 0 | N AT U R E | VO L 4 7 9 | 1 7 N O V E M B E R 2 0 1 1

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Nanoelectronic devices: taking advantage of low-dimensional materials. The case of 1D transistors based on carbon nanotubes

What is a Carbon Nanotube?

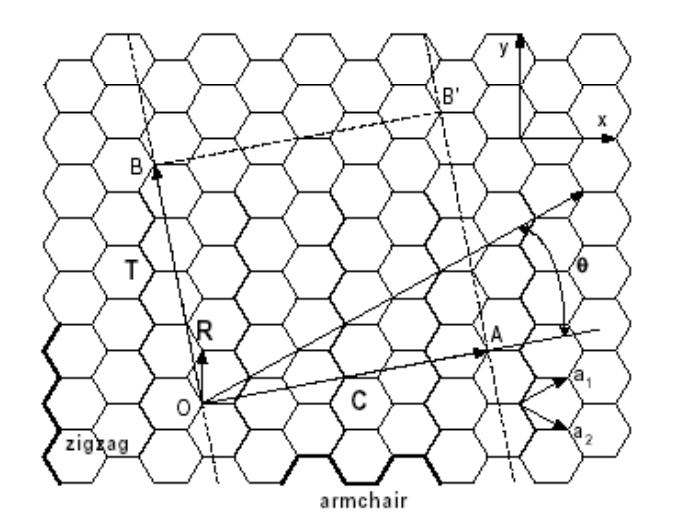
CNT is a tubular form of carbon with diameter as small as 1nm.

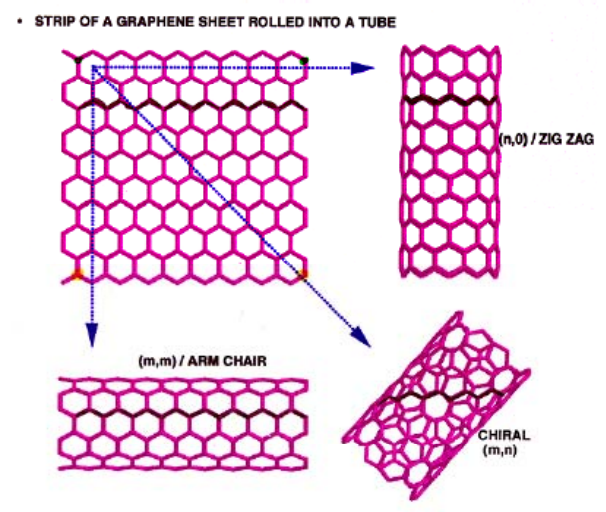
Length: few nm to microns.

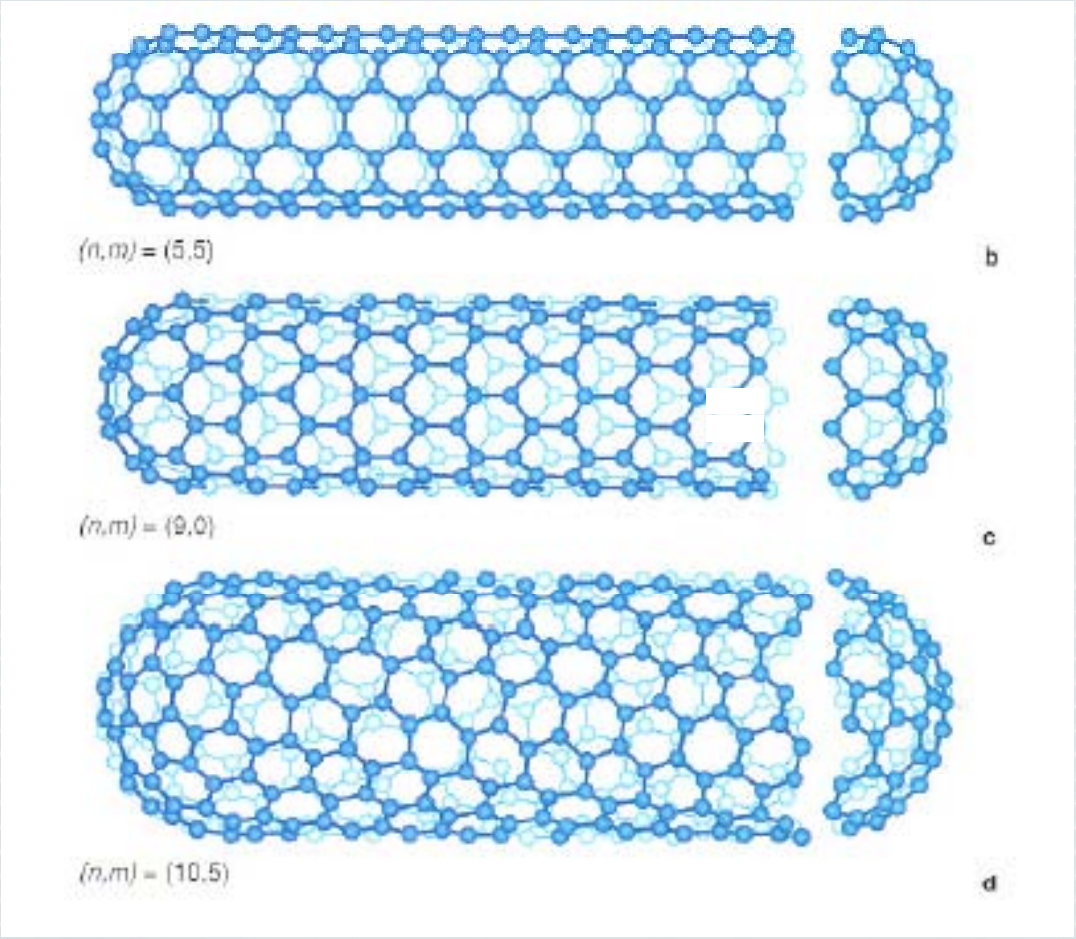
CNT is configurationally equivalent to a two dimensional graphene sheet rolled into a tube.

A CNT is characterized by its Chiral Vector: $\mathbf{C}_h = n\,\hat{a}_1 + m\,\hat{a}_2$,

$\theta \rightarrow$ Chiral Angle with respect to the zigzag axis.







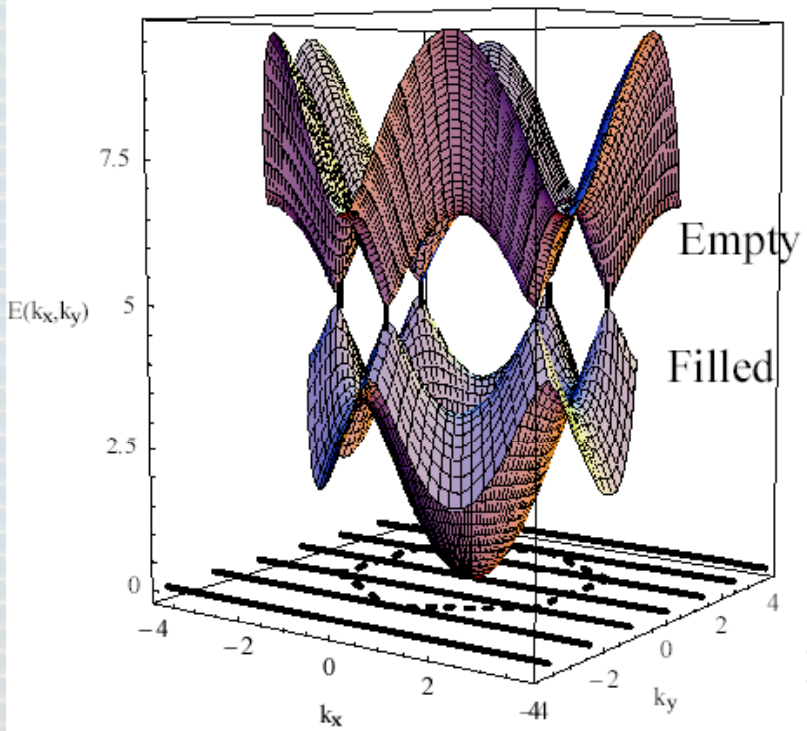
Armchair (n,m) = (5,5)
$\theta = 30°$

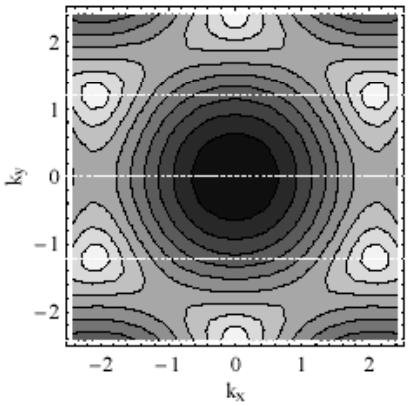
Zig Zag (n,m) = (9,0)
$\theta = 0°$

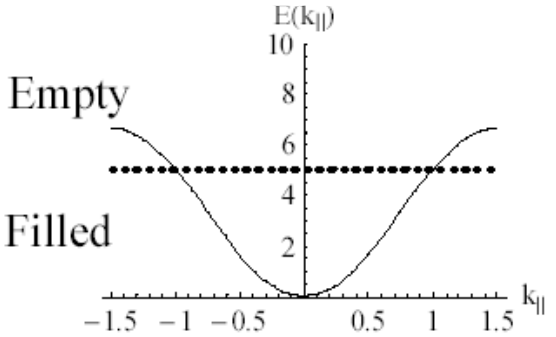
Chiral (n,m) = (10,5)
$0° < \theta < 30°$

Nanotube: Metallic

Mads Brandbyge, MIC 2003

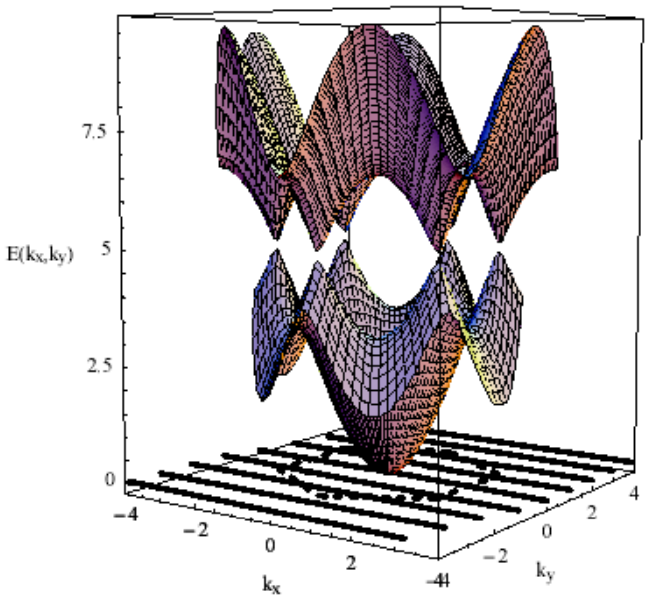


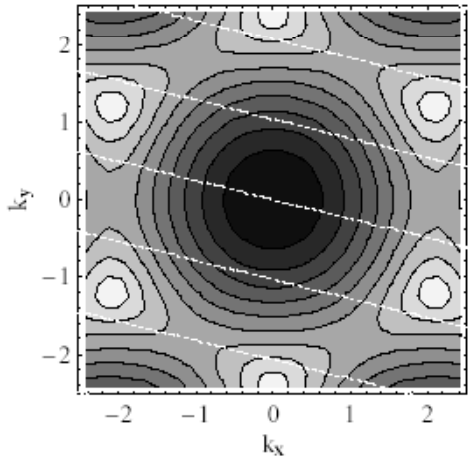


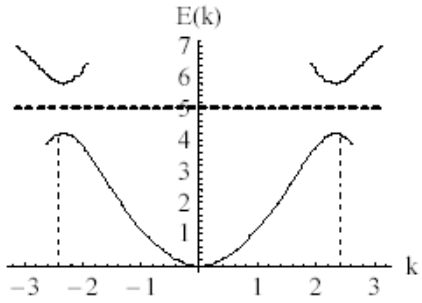


Nanotube: Semi-conductor

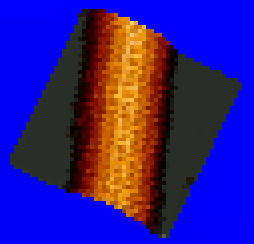
Mads Brandbyge, MIC 2003







The potential of carbon nanotubes



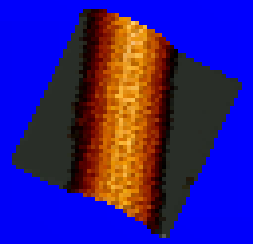
- Chemical synthesis controls the key dimensions
- Charge transport is one-dimensional
  - backscattering is strongly suppressed resulting in high "mobility" of electrons/holes

→ high I_{on} in a CNFET

  - confinement of charge inside the nanotube allows ideal control of the electrostatics

→ good suppression of SCE

The potential of carbon nanotubes



- Electron and hole transport are equal (same m*)

  → n- and p-type CNFETs are identical

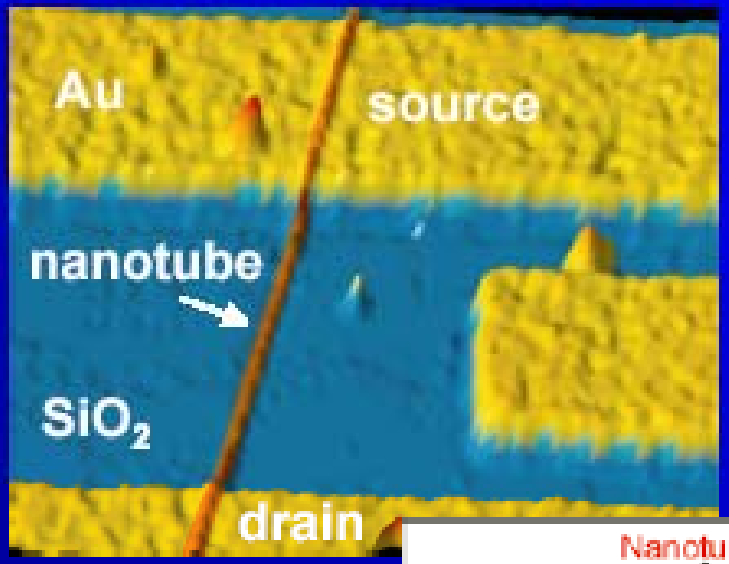
- All chemical bonds are satisfied

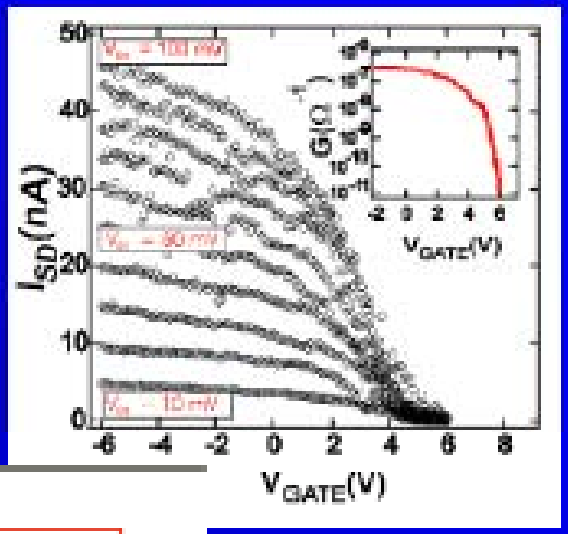
  → dielectrics other than SiO_2 can be used

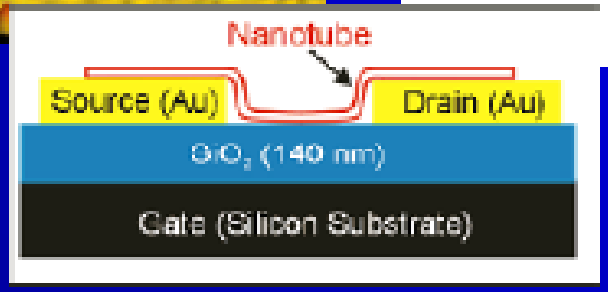
- Nanotubes can be metallic as well as semiconducting

  → an all nanotube based electronics may become possible

Carbon nanotube field-effect transistors

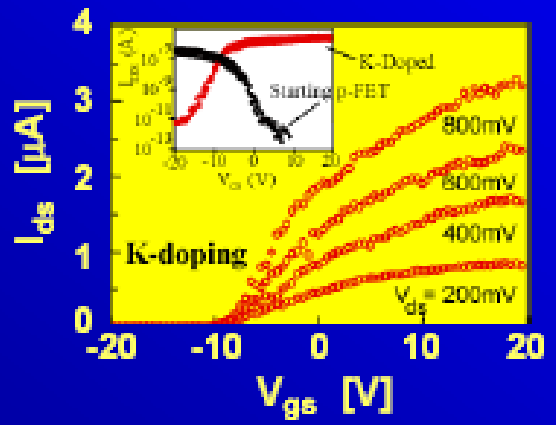


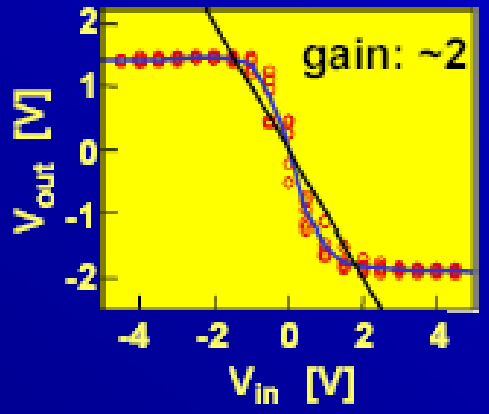


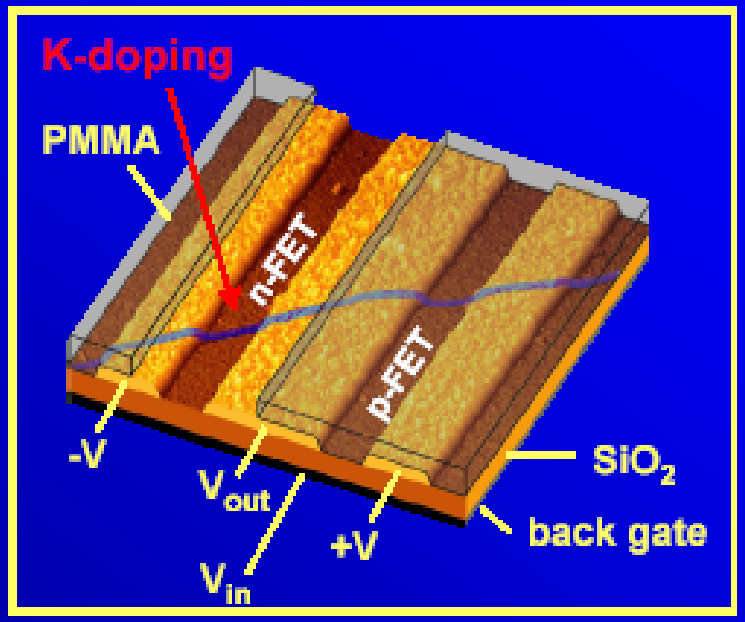


Appl. Phys. Lett. **73**, 2447 (1998)

The first intramolecular logic circuit







Nano Letters **1**, 453 (2001)

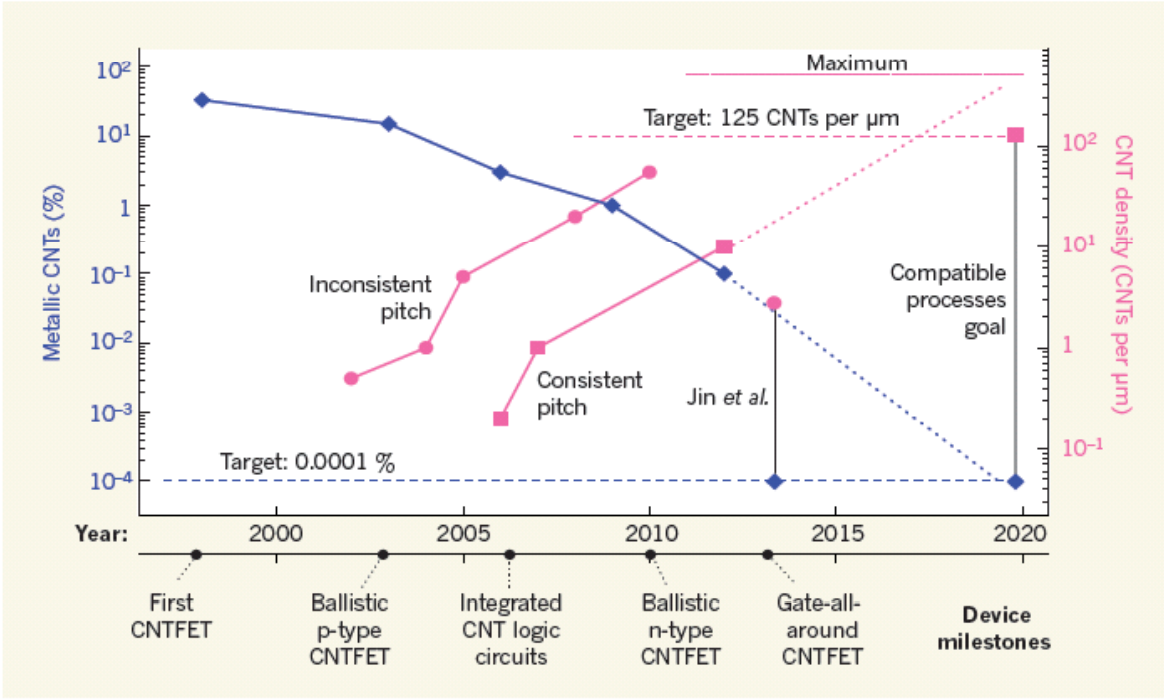


Figure 1 | Targets for carbon nanotube (CNT) transistors. The graph shows the progress in CNT transistor technology since the first demonstration of a CNT field-effect transistor (CNTFET) in 1998. The purity of semiconducting CNT material is plotted in terms of percentage of metallic CNT impurity. The placement of CNTs at a certain density is shown for both consistent and inconsistent pitch (distance) between CNTs, with the target of 125 CNTs per micrometre specified, along with the maximum of 500 CNTs per µm obtained when the CNTs are packed together without a gap between them. Trends in both purification and placement over the past decade suggest the ability to meet their targets before 2020, provided the scientific effort continues (dotted-line trajectories). Jin *et al.* introduce[1] a superb purification technique that is combined with a modest density of CNTs at an inconsistent pitch. Final approaches for achieving both less than 0.0001% of metallic CNTs and a CNT density of more than 125 CNTs per µm with consistent pitch must be compatible.

The road to carbon nanotube transistors

AARON D. FRANKLIN

2 7 J U N E 2 0 1 3 | VO L 4 9 8 | N AT U R E | 4 4 3

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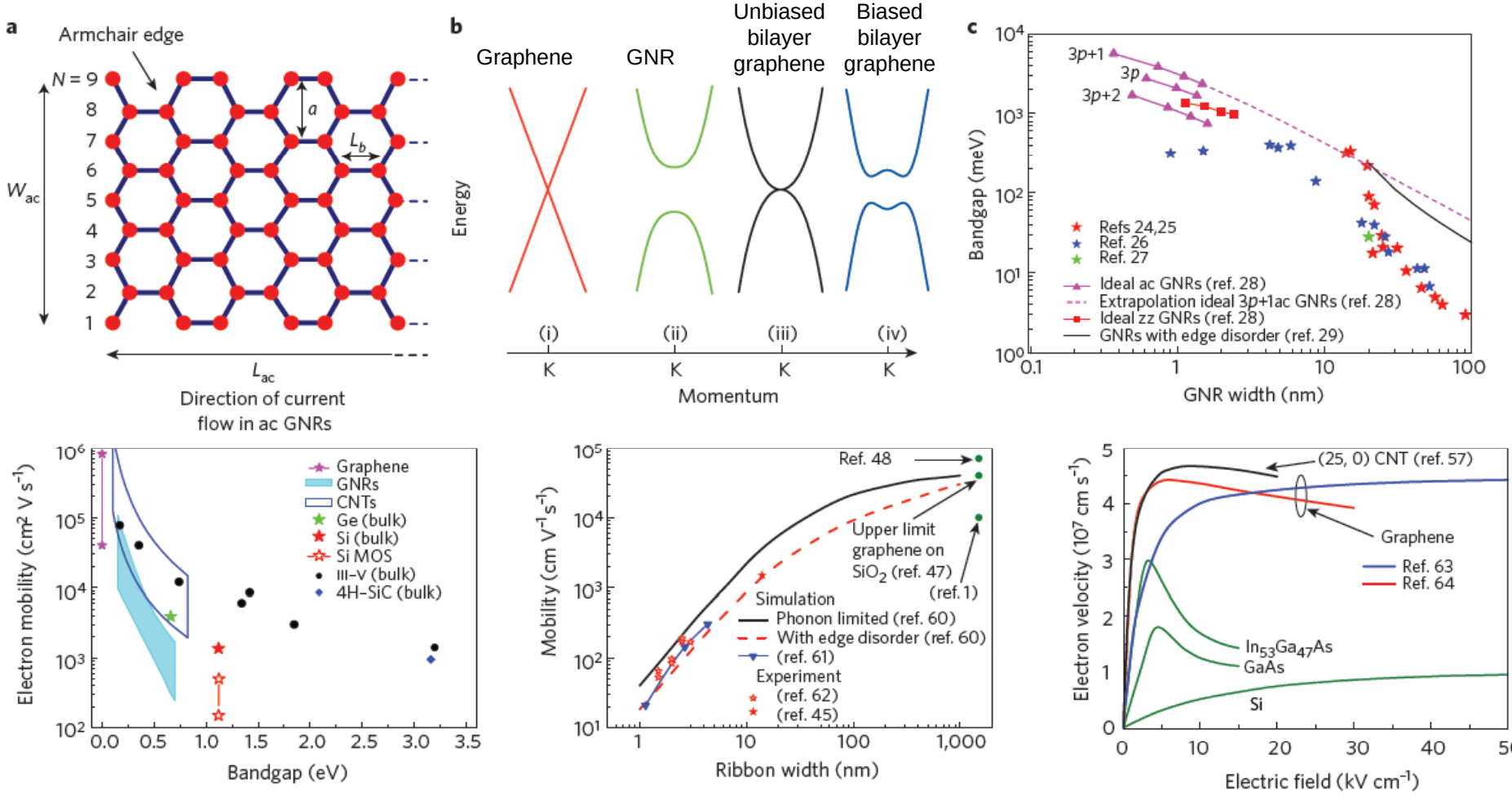
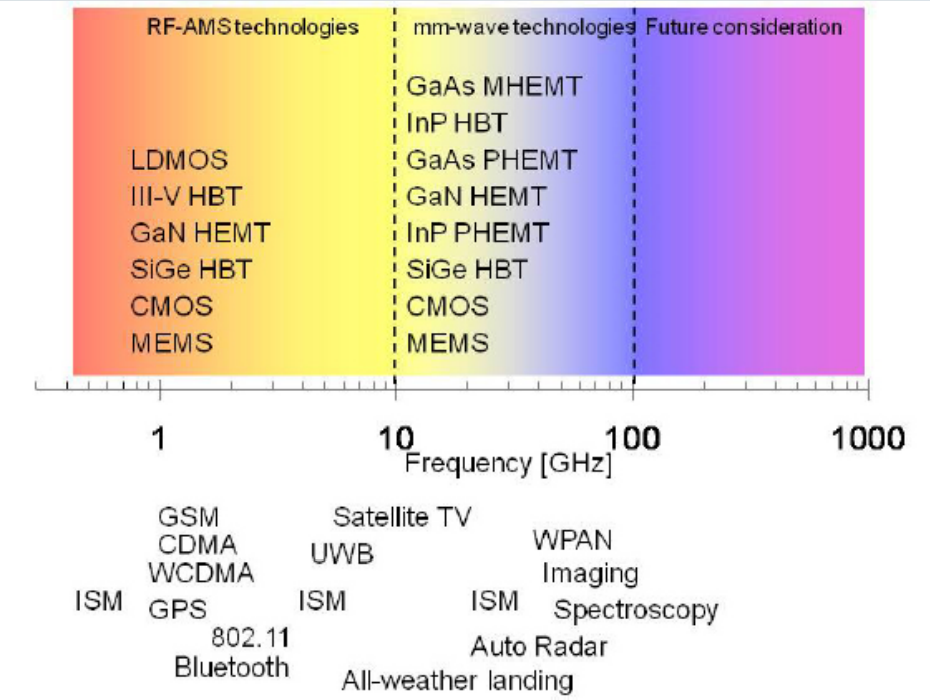
Nanoelectronic devices: taking advantage of low-dimensional materials. The case of 2D transistors based on graphene and other 2D crystals

Properties of graphene relevant for FETs

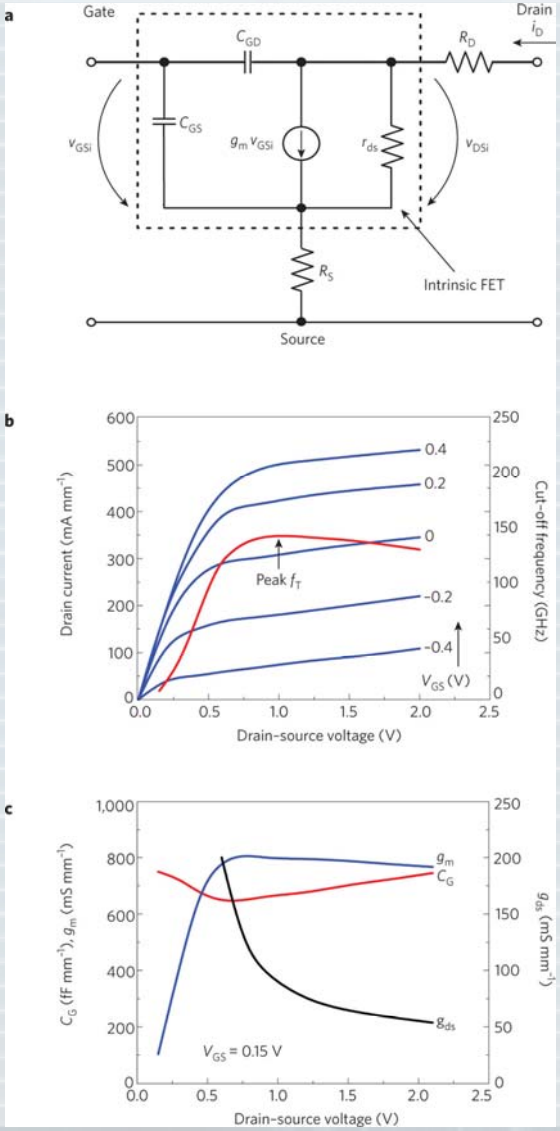


Towards THz operation

Graphene FETs present an enormous potential for **radio-frequency** and **analog** applications (cellular phones, WLANs, WPANs, radar, imaging).



Applications of RF and Analog Technologies [ITRS Roadmap]



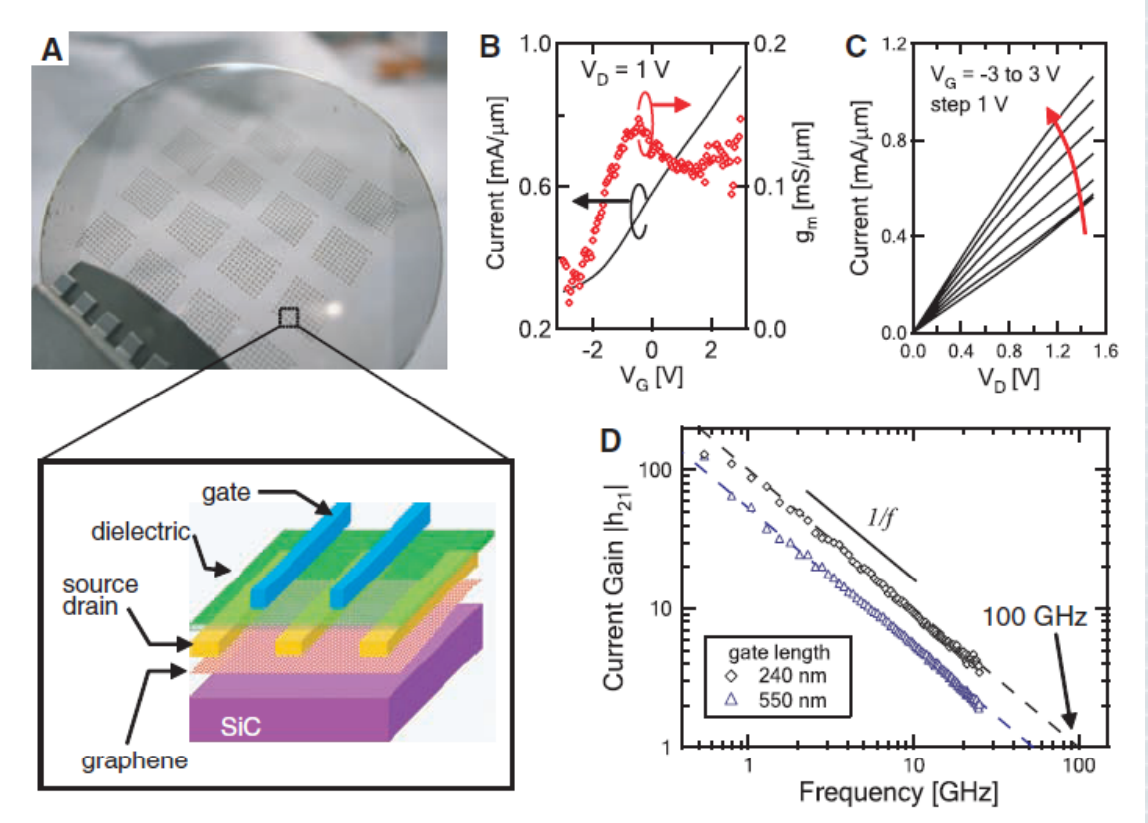
a, Small-signal equivalent FET circuit. The intrinsic transconductance, g_m, is related to the internal small-signal gate–source and drain–source voltages, v_{GSi} andv_{DSi}, whereas the terminal transconductance, g_{mt}, is related to the applied gate–source and drain–source voltages, V_{GS} and V_{DS} (Table 1 and Fig. 2b). **b**, The drain current, I_D (blue lines), at different values of V_{GS}, and the cut-off frequency, f_T (red line), both versus V_{DS} for a radiofrequency GaAs high-electron-mobility transistor[15, 16]. The cut-off frequency peaks at V_{DS} = 1 V and V_{GS} = 0.15 V. **c**, The intrinsic transconductance (blue line), the overall gate capacitance, $C_G = C_{GS} + C_{GD}$ (red line), and the drain conductance, g_{ds} ($1/r_{ds}$; black line), versus V_{DS} for the same FET.

Graphene transistors

Frank Schwierz

Nature Nanotechnology 5, 487–496 (2010) doi:10.1038/nnano.2010.89

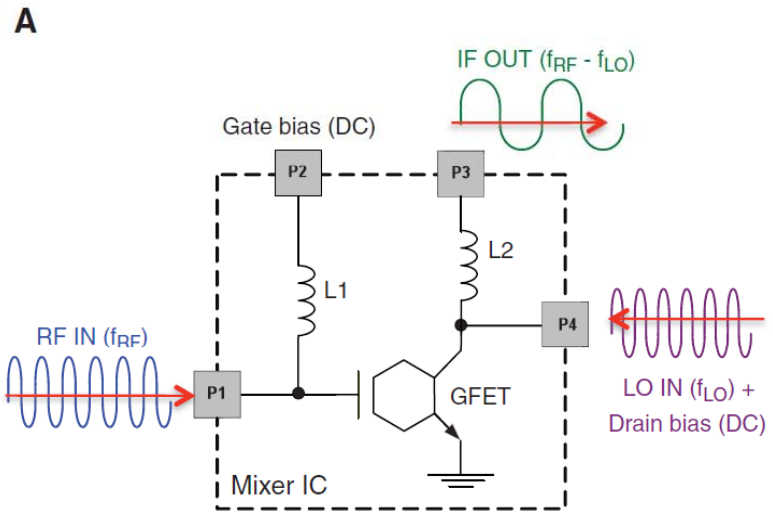
Graphene-FETs for RF applications

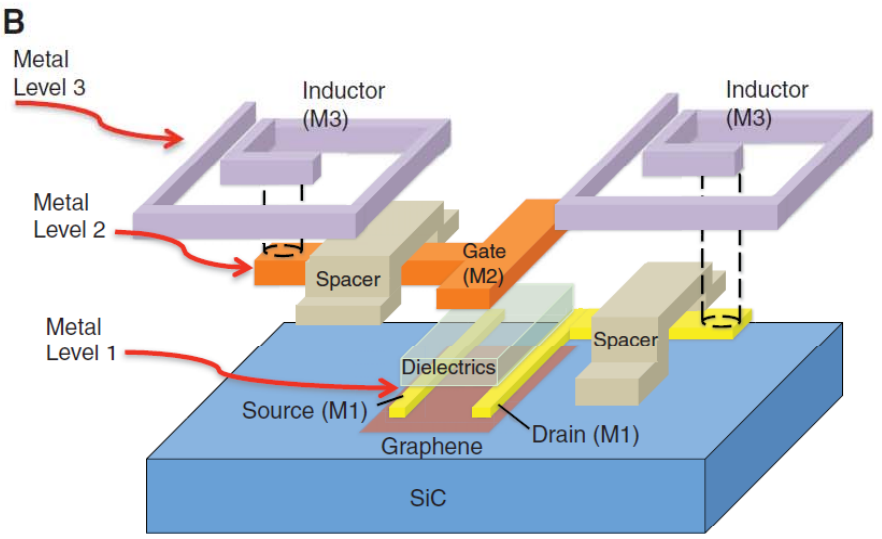


Silicon MOSFETs with a similar gate length exhibit cutoff frequencies of ~ 40 GHz

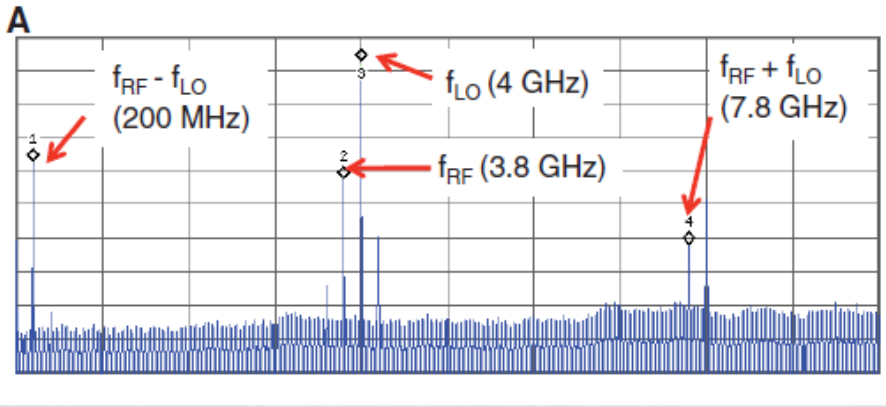
Lin et al., "100 GHz Transistors from wafer scale epitaxial graphene", Science 327 (2010)

First graphene integrated circuit: RF mixer



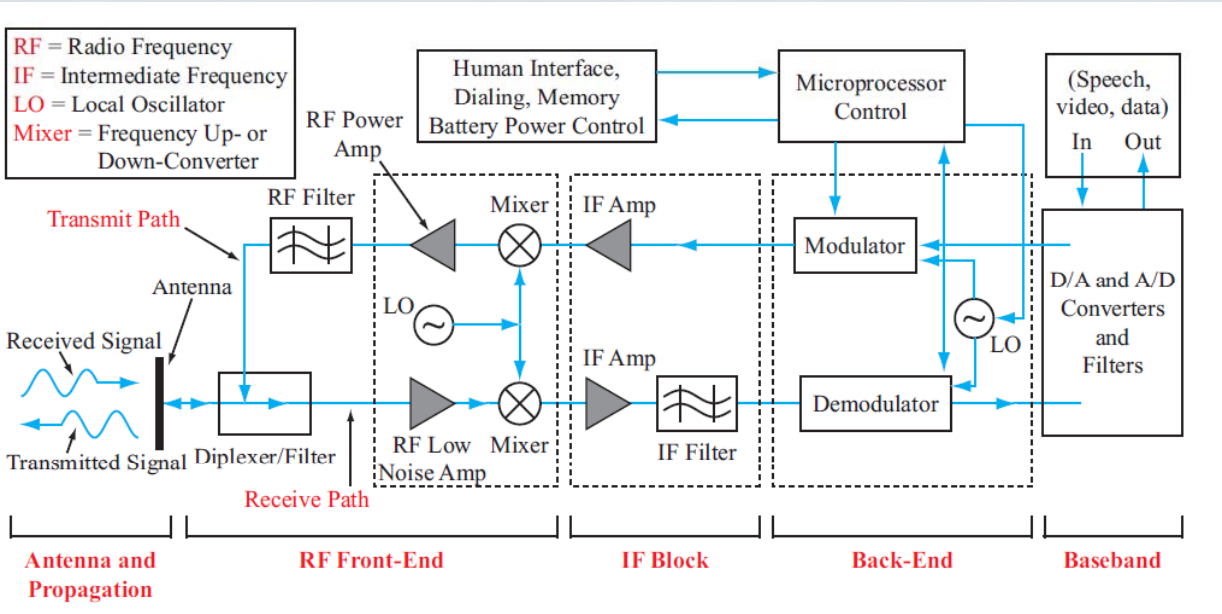


Lin et al., “Wafer scale graphene integrated circuit “, Science 332 (2011)



Cell-phone block diagram

Graphene technology could be very useful for building-up the RF Front-end of cell-phones



Other 2D atomic crystals analogues of graphene

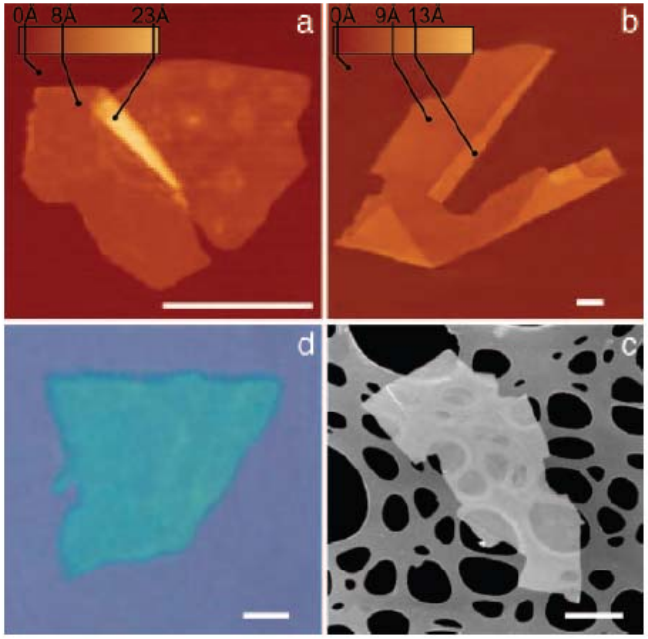


Fig. 1. 2D crystal matter. Single-layer crystallites of $NbSe_2$ (*a*), graphite (*b*), $Bi_2Sr_2CaCu_2O_x$ (*c*), and MoS_2 (*d*) visualized by AFM (*a* and *b*), by scanning electron microscopy (*c*), and in an optical microscope (*d*). (All scale bars: 1 μm.) The 2D crystallites are on top of an oxidized Si wafer (300 nm of thermal SiO_2) (*a*, *b*, and *d*) and on top of a holey carbon film (*c*). Note that 2D crystallites were often raised by an extra few angstroms above the supporting surface, probably because of a layer of absorbed water. In such cases, the pleated and folded regions seen on many AFM images and having the differential height matching the interlayer distance in the corresponding 3D crystals help to distinguish between double-layer crystals and true single sheets such as those shown here.

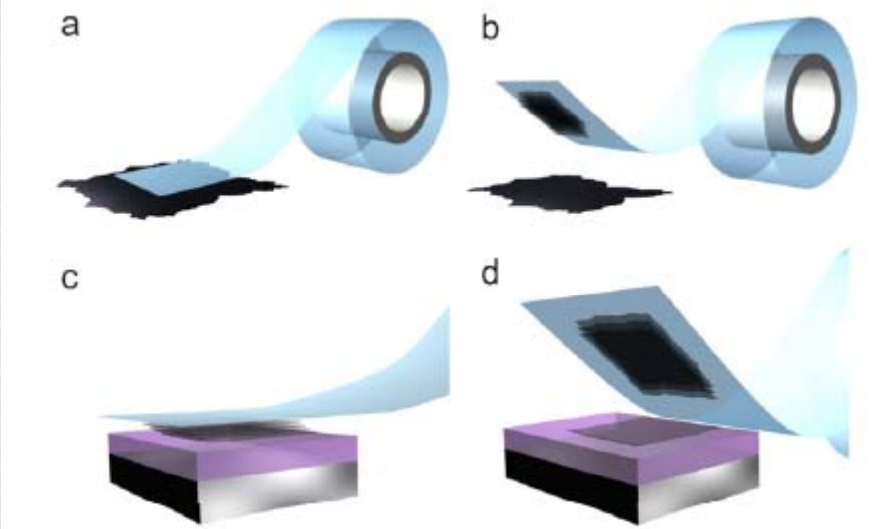


Figure 1. Micromechanical exfoliation of 2D crystals. (a) Adhesive tape is pressed against a 2D crystal so that the top few layers are attached to the tape (b). (c) The tape with crystals of layered material is pressed against a surface of choice. (d) Upon peeling off, the bottom layer is left on the substrate.

Novoselov et al., “Two dimensional atomic crystals”, PNAS 102 (2005)

Other 2D atomic crystals analogues of graphene

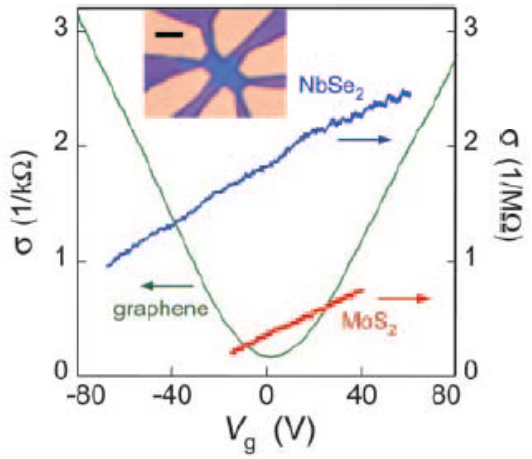
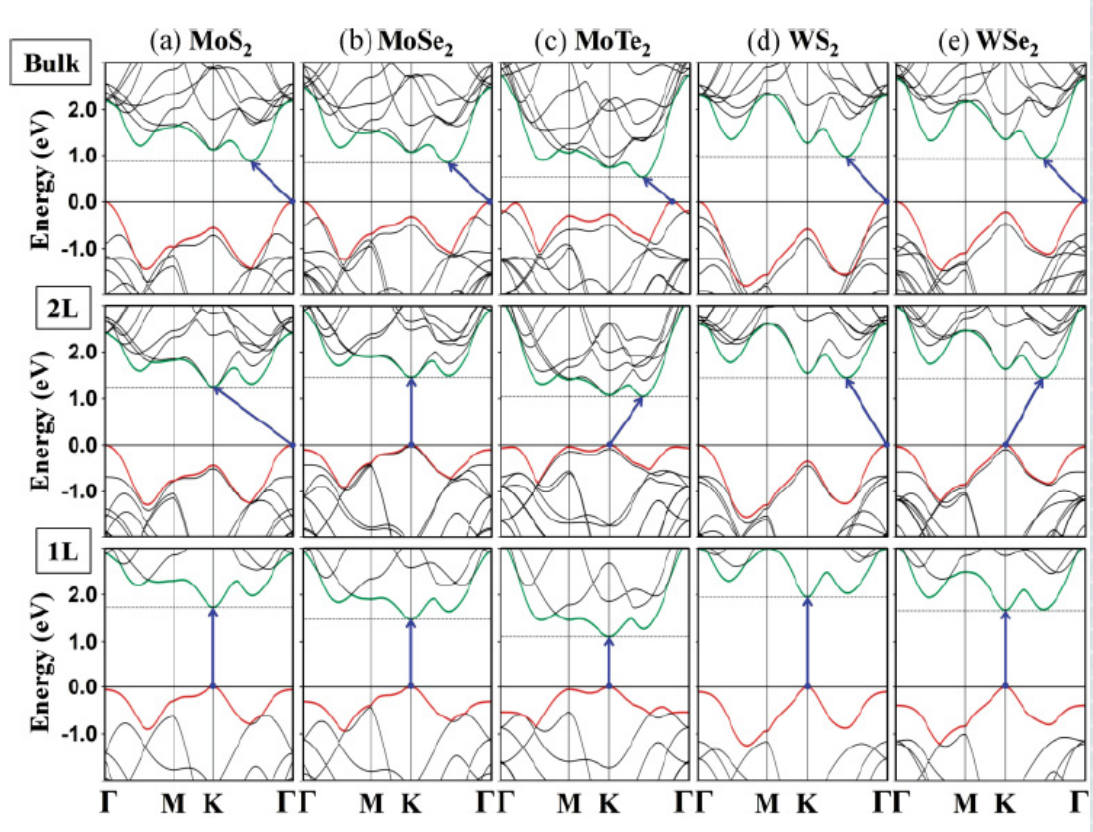


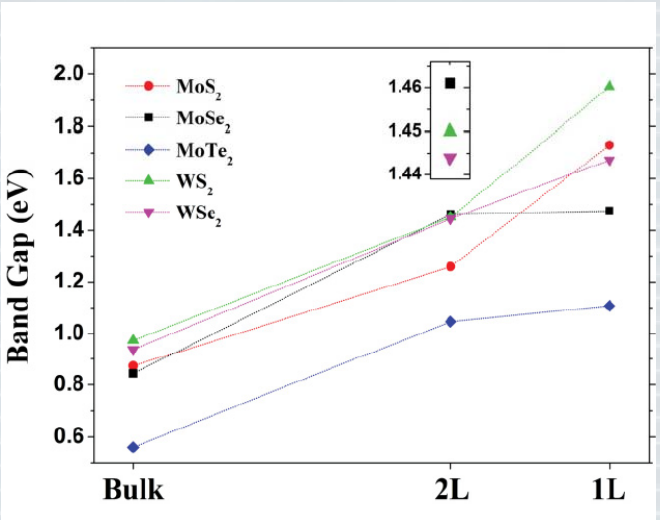
Fig. 3. Electric field effect in single-atomic-sheet crystals. Changes in electrical conductivity σ of 2D $NbSe_2$, 2D MoS_2, and graphene as a function of gate voltage are shown (300 K). (*Inset*) Our typical devices used for such measurements: It is an optical image (in white light) of 2D $NbSe_2$ on top of an oxidized Si wafer (used as a gate electrode) with a set of Au contacts. The crystal is seen as a bluer region in the center. (Scale bar: 5 μm.)

Novoselov et al., "Two dimensional atomic crystals", PNAS 102 (2005)

A family of semiconducting 2D atomic crystals: Transition Metal Dichalcogenides



MX_2 where M=Mo,W and X=S,Se,Te



W. S. Yun et al., "Thickness and strain effects on electronic structures of transition metal dichalcogenides", Phys. Rev. B 85, 033305 (2012)

First demonstration of MoS_2-FET

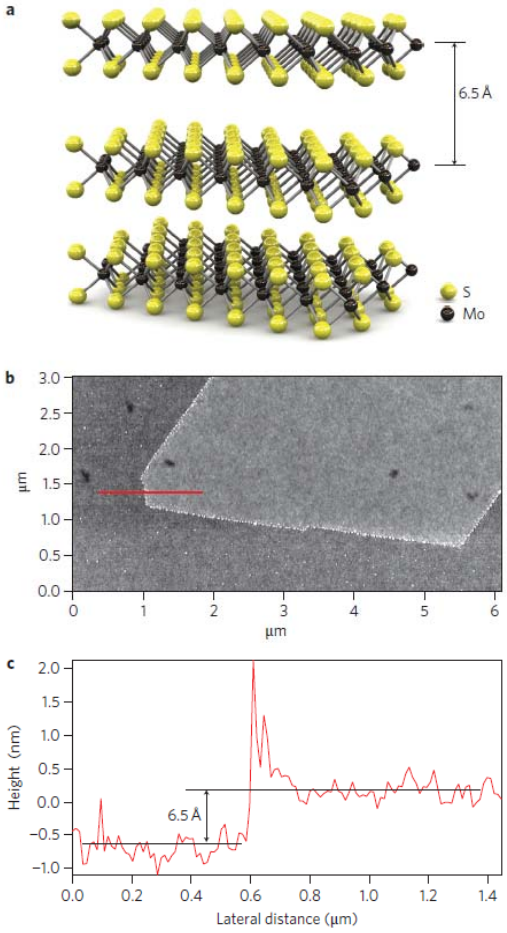


Figure 1 | Structure and AFM imaging of monolayer MoS_2. **a**, Three-dimensional representation of the structure of MoS_2. Single layers, 6.5 Å thick, can be extracted using scotch tape-based micromechanical cleavage. **b**, Atomic force microscope image of a single layer of MoS_2 deposited on a silicon substrate with a 270-nm-thick oxide layer. **c**, Cross-sectional plot along the red line in **b**.

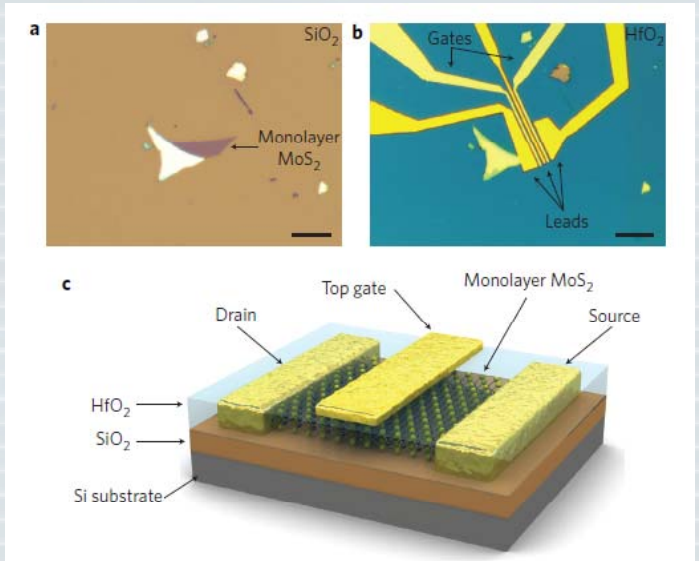
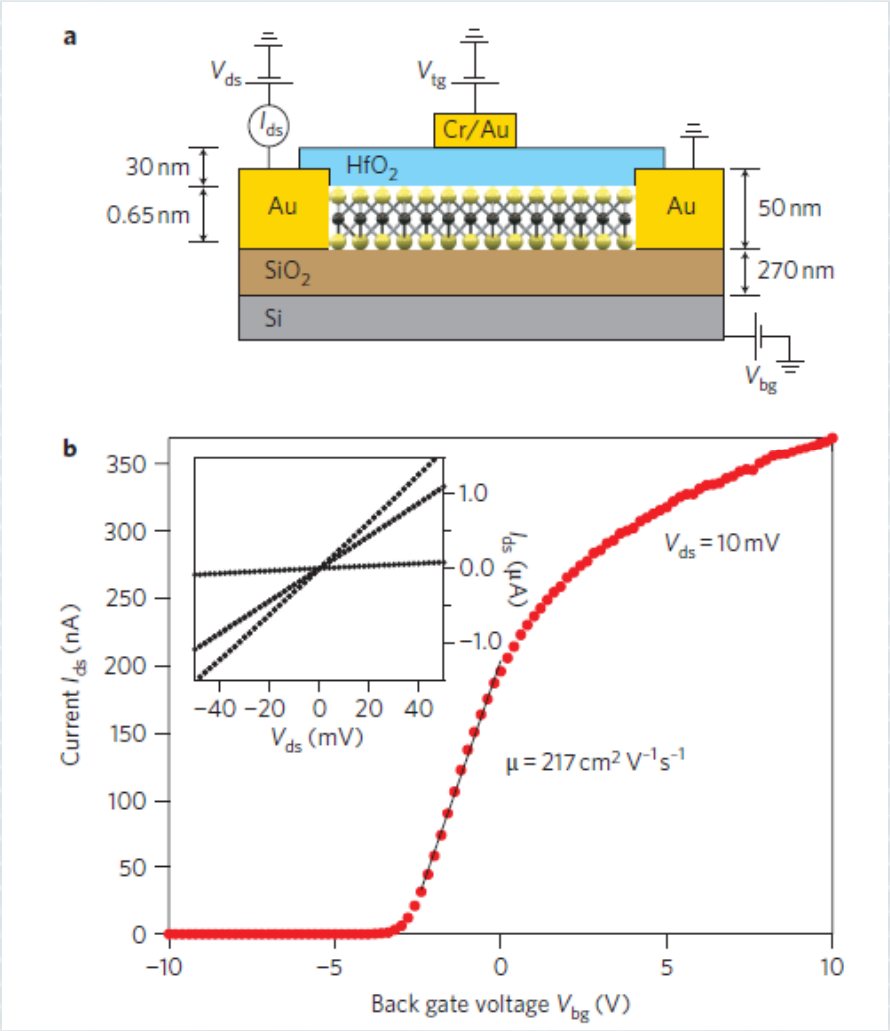
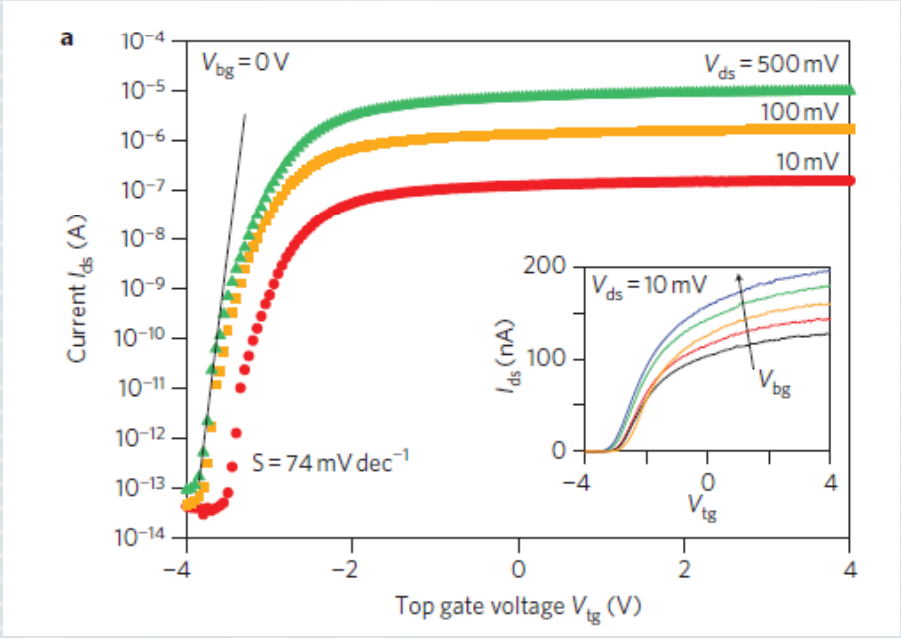


Figure 2 | Fabrication of MoS_2 monolayer transistors. **a**, Optical image of a single layer of MoS_2 (thickness, 6.5 Å) deposited on top of a silicon substrate with a 270-nm-thick SiO_2 layer. **b**, Optical image of a device based on the flake shown in **a**. The device consists of two field-effect transistors connected in series and defined by three gold leads that serve as source and drain electrodes for the two transistors. Monolayer MoS_2 is covered by 30 nm of ALD-deposited HfO_2 that acts both as a gate dielectric and a mobility booster. Scale bars (**a**,**b**), 10 µm. **c**, Three-dimensional schematic view of one of the transistors shown in **b**.

Radisavljevic et al., "Single-layer MoS_2 transistors", Nature Nanotechnology 6 (2011)

First demonstration of MoS_2-FET





2D crystal based heterostructures

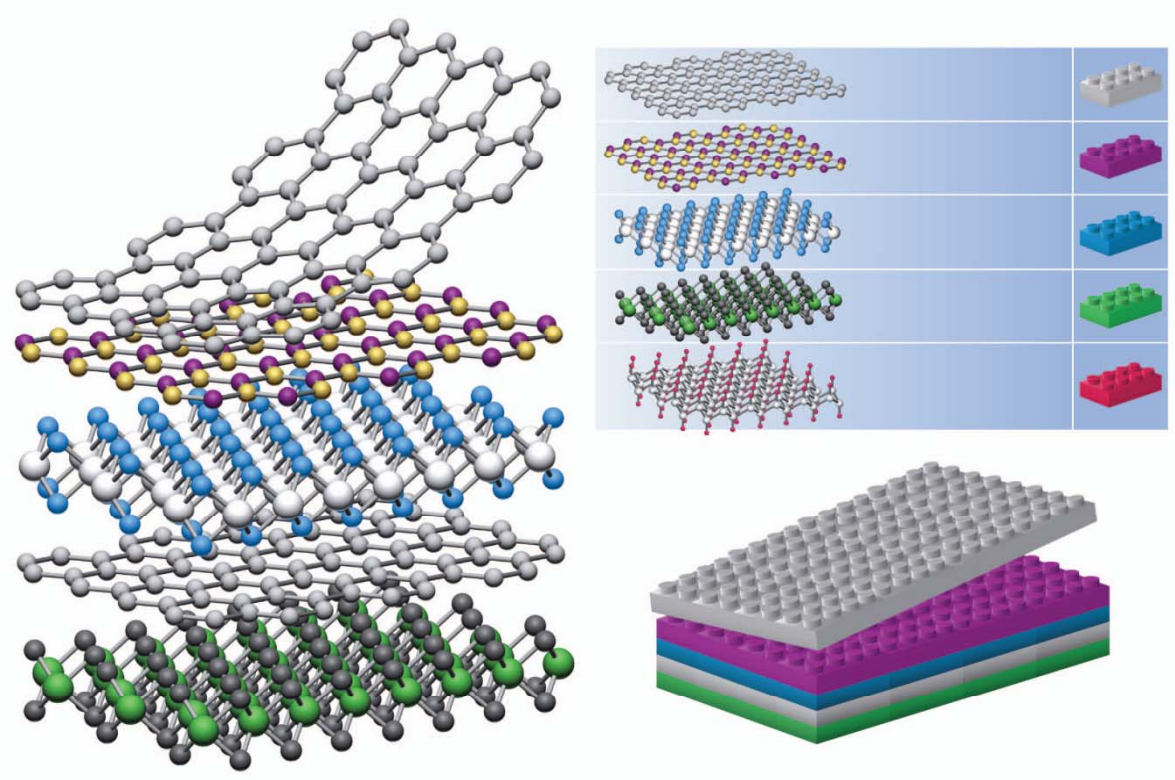


Figure 1 | Building van der Waals heterostructures. If one considers 2D crystals to be analogous to Lego blocks (right panel), the construction of a huge variety of layered structures becomes possible. Conceptually, this atomic-scale Lego resembles molecular beam epitaxy but employs different 'construction' rules and a distinct set of materials.

"Van der Waals heterostructures"
A. K. Geim & I. V. Grigorieva
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2D crystal based heterostructures

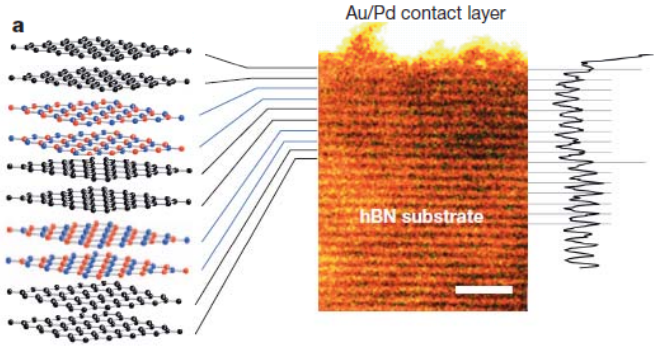

Figure 3 | State-of-the-art van der Waals structures and devices. a, Graphene–hBN superlattice consisting of six stacked bilayers. On the right its cross-section and intensity profile as seen by scanning transmission electron microscopy are shown; on the left is a schematic view of the layer sequence. The topmost hBN bilayer is not visible, being merged with the metallic contact. Scale bar, 2 nm. (Adapted from ref. 16.) b, c, Double-layer graphene heterostructures[18]. An optical image of a working device (b) and its schematics in matching colours (c). Two graphene Hall bars are accurately aligned, separated by a trilayer hBN crystal and encapsulated between relatively thick hBN crystals (hBN is shown in c as semitransparent slabs). The entire heterostructure is placed on top of an oxidized Si wafer (SiO_2 is in turquoise). The colours in b indicate the top (blue) and bottom (orange) Hall bars and their overlapping region (violet). The graphene areas are invisible in the final device image because of the top Au gate outlined by dashes. The scale is given by the width of the Hall bars, 1.5 µm.

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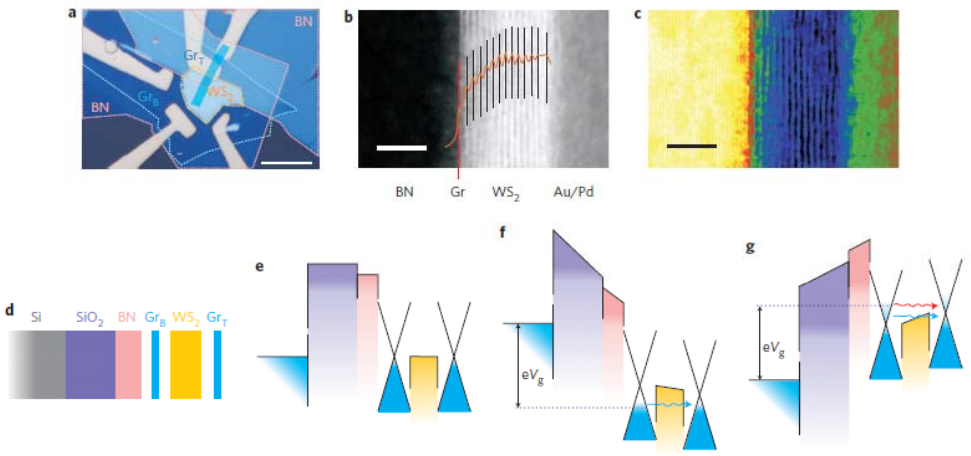

Figure 1 | Graphene-WS_2 heterotransistor. a, Optical image (scale bar, 10 μm). **b**, Cross-section high-resolution high-angle annular dark-field scanning transmission electron microscopy (HAADF STEM) image (scale bar, 5 nm). **c**, Bright-field STEM image (scale bar, 5 nm). **d**, Schematic of vertical architecture of transistor. **e**, Band diagram corresponding to no V_g and applied V_b. **f**, Negative V_g shifts the Fermi level of the two graphene layers down from the neutrality point, increasing the potential barrier and switching the transistor OFF. **g**, Applying positive V_g results in an increased current between Gr_B and Gr_T due to both thermionic (red arrow) and tunnelling (blue arrow) contributions.

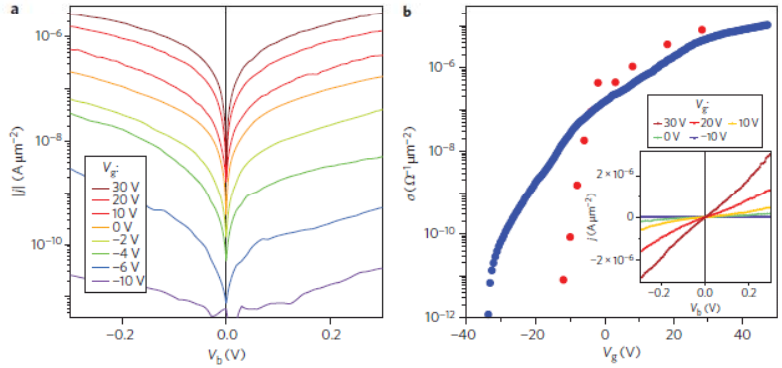

Figure 2 | Room-temperature tunnelling transport measurements in the graphene-WS_2 transistor. a, *I*–*V* plots for different V_g (semi-logarithmic scale). **b**, Red circles: zero-bias conductivity as a function of gate voltage (measured as the slope of the *I*–V_b curve at zero V_b). Blue circles: conductivity measured at $V_b = 0.02$ V as a function of gate voltage. Inset: *I*–*V* at different V_g (linear scale). $T = 300$ K. Device active area, 0.25 μm^2.

Georgiu et al., "**Vertical field-effect transistor based on graphene–WS2 heterostructures for flexible and transparent Electronics**" NATURE NANOTECHNOLOGY | VOL 8 | FEBRUARY 2013 |

Current 2D crystal library

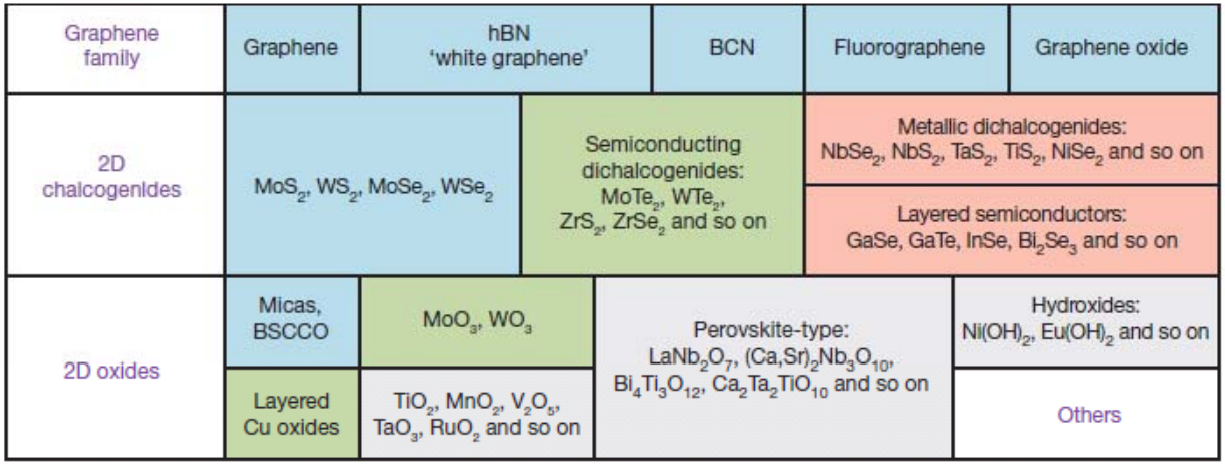

Figure 2 | Current 2D library. Monolayers proved to be stable under ambient conditions (room temperature in air) are shaded blue; those probably stable in air are shaded green; and those unstable in air but that may be stable in inert atmosphere are shaded pink. Grey shading indicates 3D compounds that have been successfully exfoliated down to monolayers, as is clear from atomic force microscopy, for example, but for which there is little further information. The data given are summarized from refs 6–11, 42 and 55. We note that, after intercalation and exfoliation, the oxides and hydroxides may exhibit stoichiometry different from their 3D parents (for example, TiO_2 exfoliates into a stoichiometric monolayer of $Ti_{0.87}O_2$; ref. 8). 'Others' indicates that many other 2D crystals—including borides, carbides, nitrides and so on—have probably been[7–11] or can be isolated. BCN, boron carbon nitride.

Graphene Flagship project

Graphene appointed an EU Future Emerging Technology flagship. The European Commission has chosen *Graphene* as one of Europe's first 10-year, 1000 million euro FET flagships. The mission of Graphene is to take graphene and related layered materials from academic laboratories to society, revolutionize multiple industries and create economic growth and new jobs in Europe.

http://www.graphene-flagship.eu/GF/index.php